Catapult
High Level Synthesis Platform

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Introducing the Catapult HLS Platform

The Only Complete Design and Verification Platform for C++/SystemC

- High Quality RTL Synthesized from C/C++/SystemC
- Verification for C/C++/SystemC HLS Design and Production flow into RTL
- PowerPro under-the-hood for Best Power Optimized RTL
- Physically-Aware using Oasys RTL Synthesis Engine
Catapult HLS – Design at a Higher Level

- Generate high quality RTL from high level descriptions
  - Designs are correct-by-construction
  - Both ASIC and FPGA targets from the same source code
  - Target technology aware micro architecture generation
  - Generate synthesis scripts for major logic synthesis tools

- Seamless functional verification flow from C to RTL
  - Built-in C-level design and coverage checks
  - C-to-RTL formal equivalence checker
  - RTL co-simulation with major logic simulators

- Integrated PowerPro ASIC Estimation & Optimization technology

- Key applications have already moved to HLS
  - Video Compression/Decompression (H.265/HEVC, VP9)
  - Image Processing (Mobile/4k/Ultra HD/3D)
  - Wireless/Wireline (Bluetooth, 5G, 802.11, Gb optical, DOCSIS)
Language Freedom

- The only ASIC/FPGA HLS tool to support both C++ and SystemC

- Supports all popular SystemC abstractions
  - Untimed, Loosely-timed, Cycle-accurate
  - SC_METHOD and SC_CTHREAD

- Applicable to all use cases
  - Exploration and Implementation
  - Control Logic and Algorithms

- Flexibility to use the best language for a team, project or application

- Teams will typically select one language, but company may use both
Catapult Enables Re-Use between FPGA and ASIC

- Enable designers to bring algorithms into high-speed HW/FPGA for fast Proof of Concept or demonstrator

- Key IP blocks reused from FPGA to ASIC to save months of redevelopment

- Any ASIC library can be characterized to HLS

- Easy switching between eFPGA and ASIC

- Same C code can be retargeted for different market/application within days

High speed FPGA and ASIC
Catapult Enables Designers to Verify Functionality at C-level and Fit into Existing RTL Methodology

- Re-Use/Refine from functional reference model
- Verify and debug HLS source at 500X performance
- Generate quality RTL quickly that fits into known RTL methodologies
Catapult – The Only Low Power HLS Solution

- Integrated Early RTL Power Estimation with PowerPro “under the hood”

- Explore µArchitectures with constraints
  - Evaluate PPA alternatives for each design
  - Frequency exploration
  - Resource sharing
  - Memory access minimization
    - Banking & interleaving

- Generate power optimized RTL with Catapult Ultra
  - Automatic Optimization with PowerPro Engine
  - Converge rapidly on optimal solution

- Only Catapult Ultra has this integrated technology
COSIDE® – Catapult Integration

- Seamless transition of DCORE from COSIDE® to Catapult HLS synthesis environment
- HLS synthesis scriptable
  - push-button HLS synthesis down to RTL
  - push-button FPGA synthesis for Rapid Prototyping
- Reuseable COSIDE® verification scenarios, regression suite
  - RTL verification in Catapult using COSIDE® testbench environment with analog functionality