COSIDE® supported Multi Simulator SystemC usage – from Customer till Design

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Scope of COSIDE® (supported) Use Cases

1 Concept Feasibility & Verification

2 Co-Simulation

3 Customer Model

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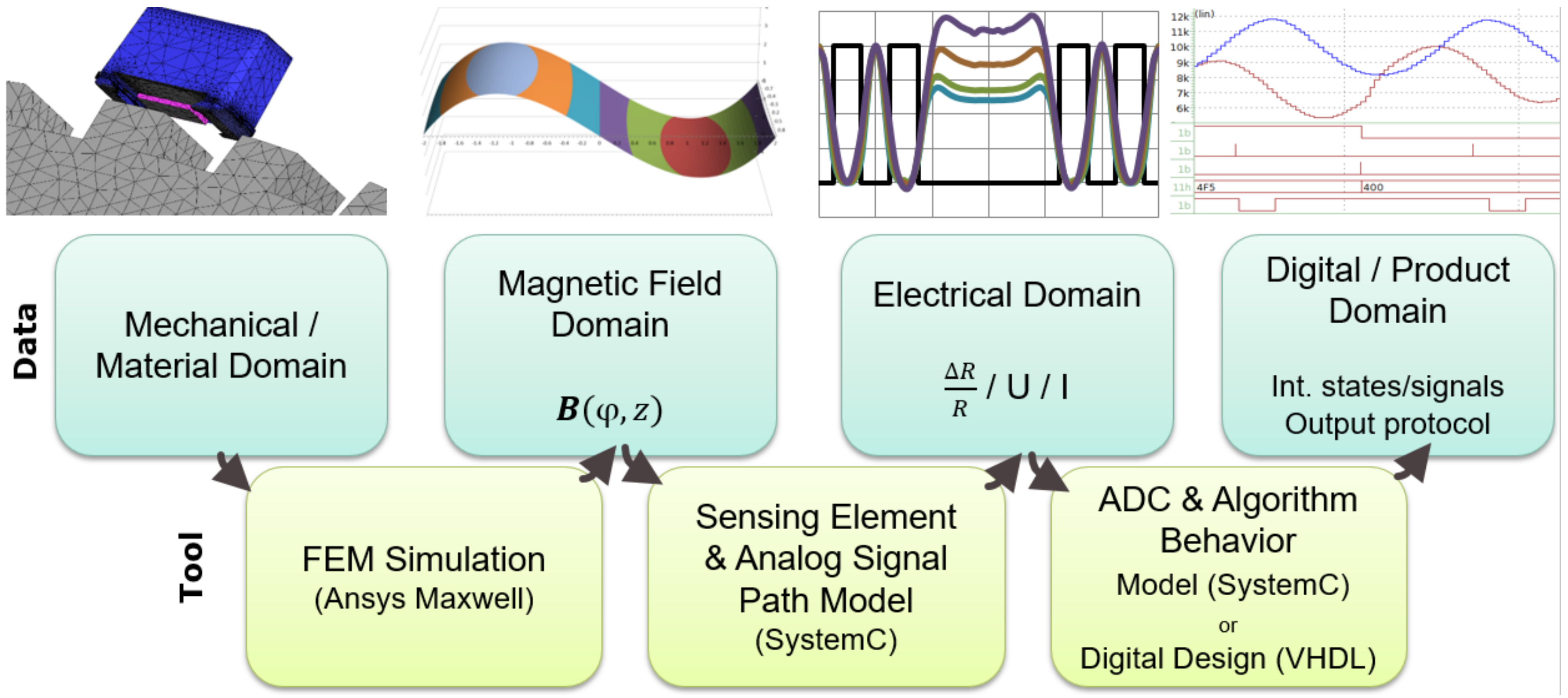
1. **Concept Feasibility & Verification**
2. Co-Simulation
3. Customer Model

Concept Feasibility & Verification

- Provide stimuli / model test cases
- Check Feasibility of REQs – static and dynamic
- Compare different architectures / algorithms
- Pre-evaluate model behaviour against modelled (state machine) target behaviour in SystemC to ease results handling & allow small file interfaces
- Run regression with built-in frameworks or allow usage of script-language for „outer layer" using file interfaces
- Verify Concept & give an early indication about target-application-performance

Concept Feasibility & Verification

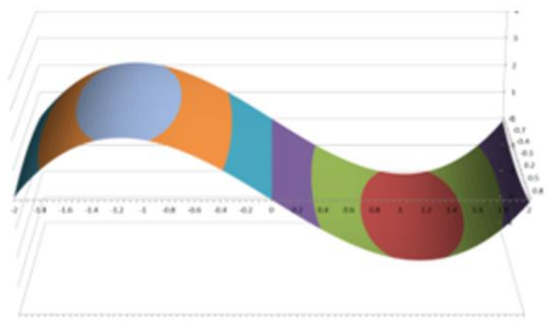
› Simulation chain example – Magnetic Sensor, focus on digital behaviour



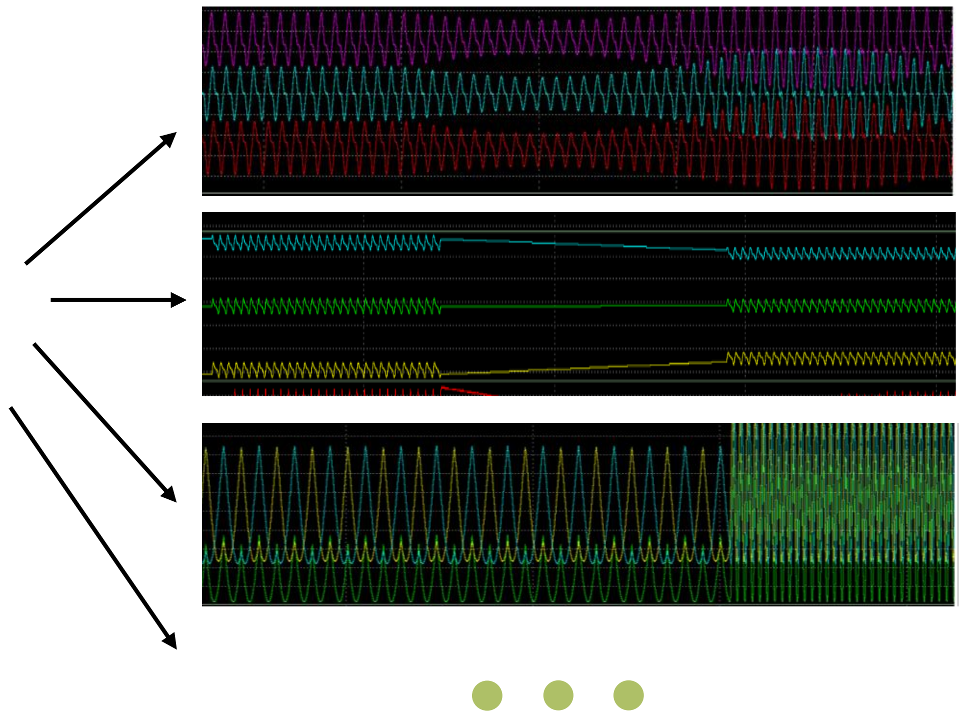
Concept Feasibility & Verification

› Simulation chain example – Test case creation from Stimuli

Magnetic field in pre-defined parameter space



Magnetic fields in test case sequence over time



Read pre-simulated stimuli from binary files and do expensive test case calculations in SystemC (significantly more efficient)

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Co-Simulation

› Compare Concept model against implementation

› Provide executable specification to design

› Identify deviations/bugs by comparison (depending on model complexity even bit/clk-wise comparsion possible)

› Re-Use SystemC TB

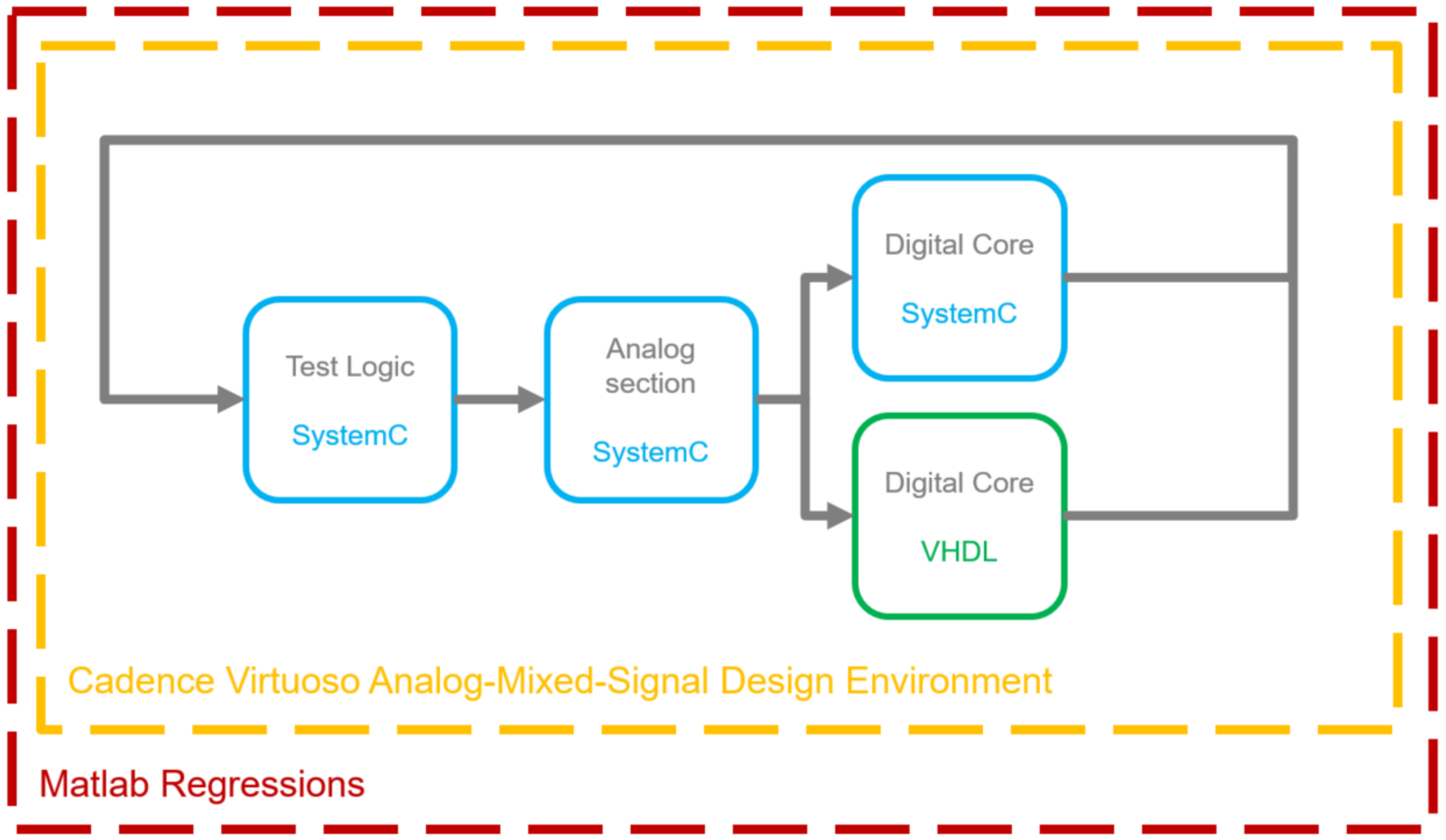
› Currently two Flows in use

  – CCB - Cadence® on top (more flexible regarding supported languages)

  – Direct HDL simulation using sc_main on top (flexible in TB usage)

Co-Simulation

› Example Setup



Co-Simulation

- COSEDA®-Cadence®-Bridge
  - Generate Interfaces/Symbols for Cadence® ADE using COSIDE® – even generate Netlists from schematics
  - Compile Incisve®/Xcelium™ libraries
  - Link COSIDE®-generated files in Cadence®
  - Run Concept model/Design in parallel or replace blocks on arbitrary level

Co-Simulation

- Incisive® /Xcelium™ Simulation
  - Provide Interface from SystemC to HDL
  - Header file can be integrated in schematic without implementation and work as a link to an HDL-Wrapper
  - Provide script to parse sc_main arguments, provide useful Incisive®/Xcelium™ settings and include COSIDE® libraries
  - COSIDE® is going to provide the functionality to generate this header files and will allow the generation of executables handling the scripting above, which is currently done manually
  - Run Concept model/Design in parallel or replace blocks on arbitrary level

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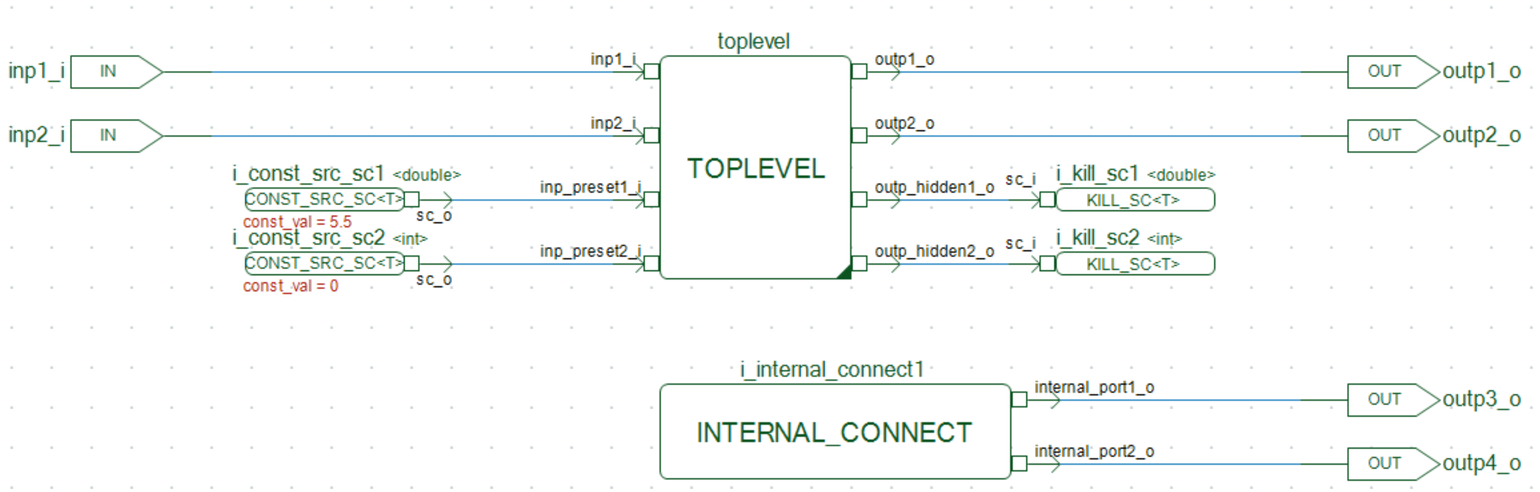
Customer Model

- Provide useful interface adaptations to ease model handling & provide „spys" on lower levels
- Generation of SIMULINK® BB model
- Allow early integration tests
- Give customer performance indication already in early development state

Customer Model

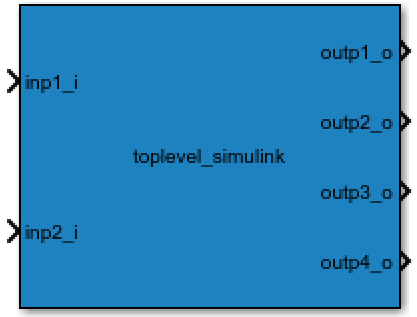
› Useful interface adaptations
  - Define subset of inputs
  - Hide subset of model outputs
  - Add internal signals to interface



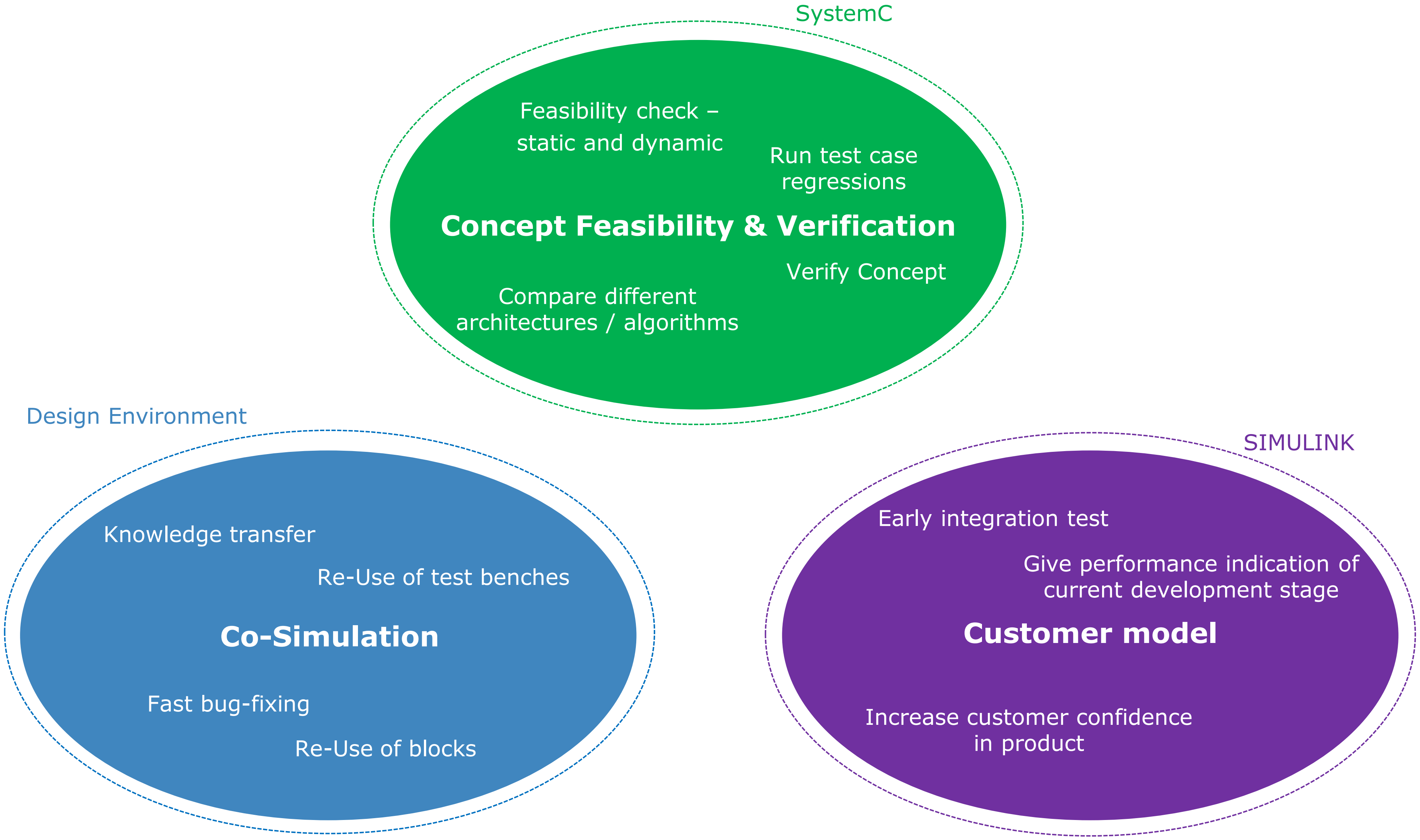
Use Schematic and get maintainance for free!

Customer Model

- Generate SIMULINK® model
  - Apply COSIDE® Coupling functionality on target xml
  - Update model via make all (if the interface does not change, no maintainence necessary)
  - Arbitrary number of customized models via schematics handleable
  - Parameter handling also possible via masks
  - Ready for SIMULINK TB



Conclusion of COSIDE®-supported Use-Case Flows (scope of this presentation)


SystemC
Feasibility check – static and dynamic
Run test case regressions
Concept Feasibility & Verification
Verify Concept
Compare different architectures / algorithms
Design Environment
Knowledge transfer
Re-Use of test benches
Co-Simulation
Fast bug-fixing
Re-Use of blocks
SIMULINK
Early integration test
Give performance indication of current development stage
Customer model
Increase customer confidence in product

Part of your life. Part of tomorrow.