

HiL Firmware Prototyping Using an COSIDE[®] Asynchronous Motor Model

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1. Introduction

- Effektiv Project
- HiL Intro
- Example System
- Motivation: Why HiL?

2. Tooling

3. Failure Injection

4. Demonstrator

Research project Effektiv

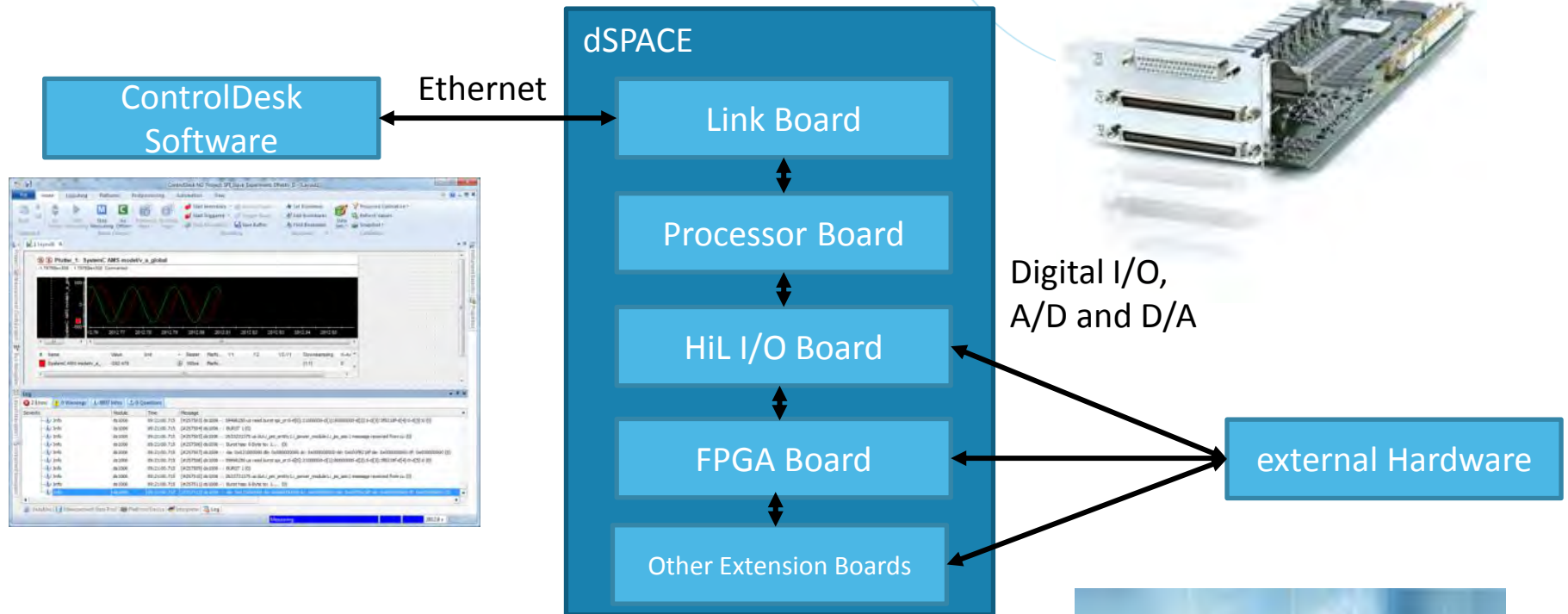


- Virtual stress tests for intelligent motion control systems
- German BMBF research project
- Fraunhofer as subcontractor of SIEMENS
- Consortium



- Our Focus: Hardware in the Loop Simulations with SystemC AMS

HiL Introduction



- **Other Extension Boards for specific needs (high speed or precision) or additional interfaces (LIN ...) available**



Source: dSPACE

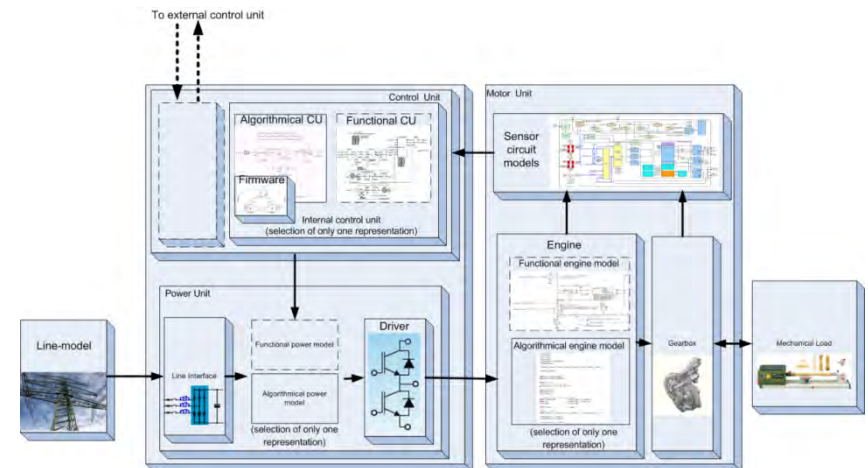
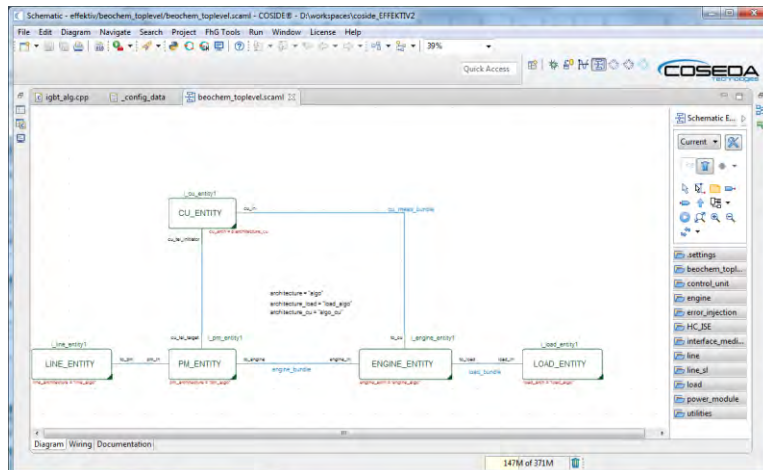
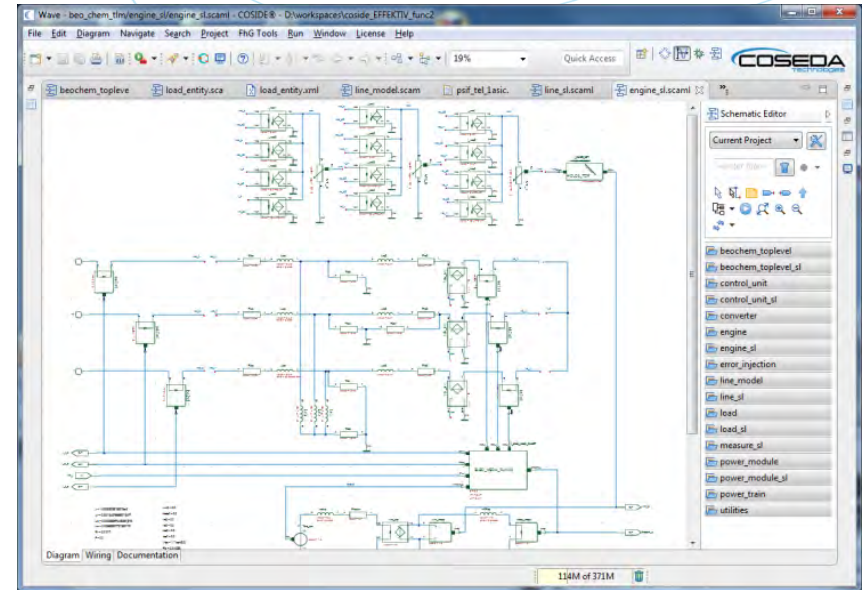
- **Debug** – Accessibility and Traceability from Signals for error root cause analysis
- **Speed/Detail** – Tradeoff between model speed vs detail level
- **Failure Injection** – Possibility to manipulate expected behavior to evaluate system robustness

Pure Virtual	Real Hardware	Mixed (HiL)
<ul style="list-style-type: none">• Debug ++• Environment model (+)<ul style="list-style-type: none">- Virtual Sensors• Speed/Detail --• Failure Injection ++	<ul style="list-style-type: none">• Debug --• Environment model (+)<ul style="list-style-type: none">- Hardware Sensor• Speed/Detail ++• Failure Injection --	<ul style="list-style-type: none">• Debug +• Environment model (++)<ul style="list-style-type: none">• Both possible• Speed/Detail +• Failure Injection +

Example System

■ Motion-Control-System

- Control Unit (CU)
- Power Module (PM)
- Engine
- Load
- Line-Module



Why HiL? (2)

- **Task: Firmware development on the Control Unit (CU) for an asynchronous Motor**
- **Setup:**
 - CU as prototypes or hardware revision
 - SystemC AMS of PM, engine, load, line model running on dSPACE
- **Advantages:**
 - Realistic Firmware environment for CU through the use of real hardware
 - Use of proven failure injection models within SystemC AMS
 - Enables also the exploration of critical corner cases, which would destroy the real hardware

1. Introduction

2. Tooling

- SystemC AMS on dSPACE
- Tooling Environment

3. Failure Injection

4. Demonstrator

SystemC-AMS Executable



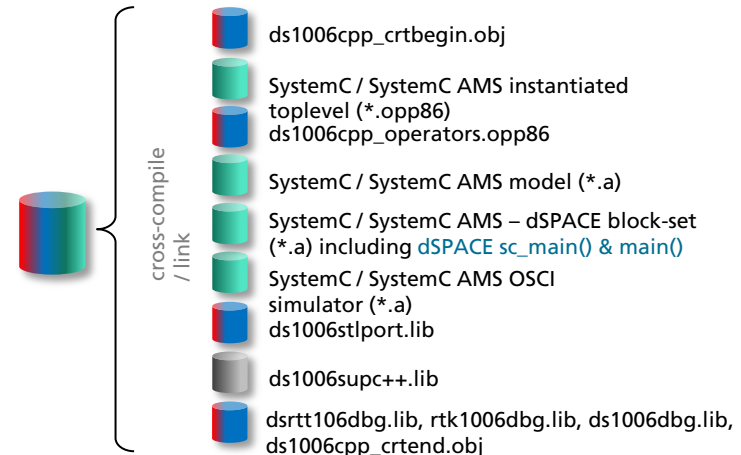
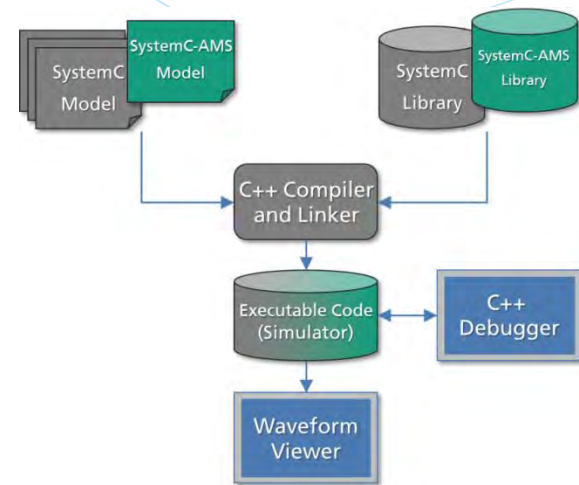
SystemC AMS Model

SystemC AMS Model
with dSPACE wrapper

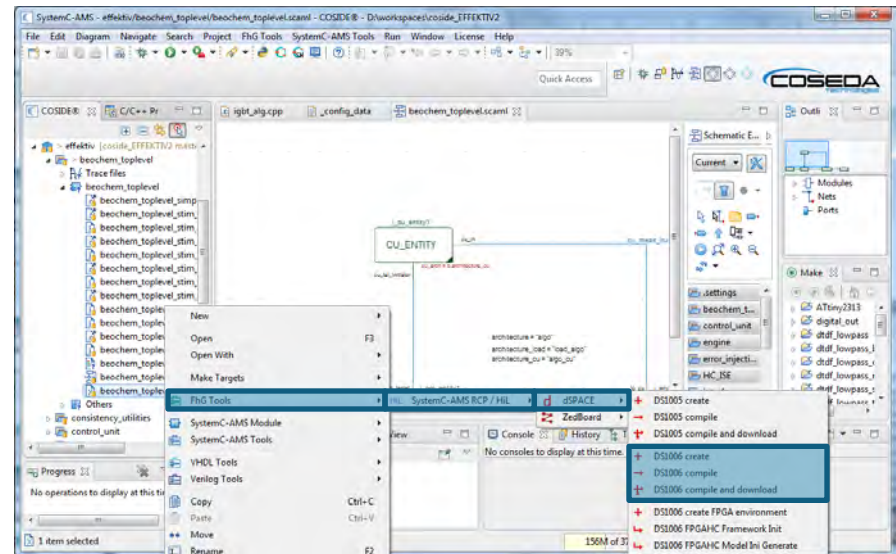
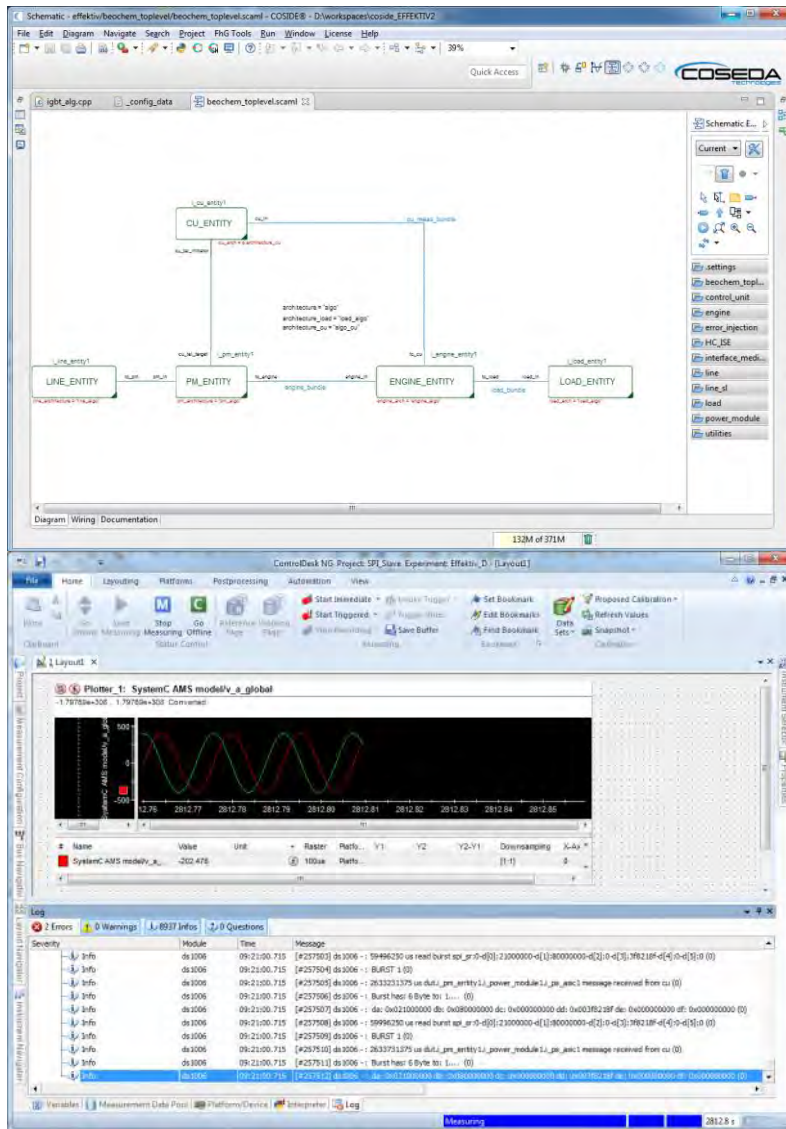
dSPACE



Source: dSPACE

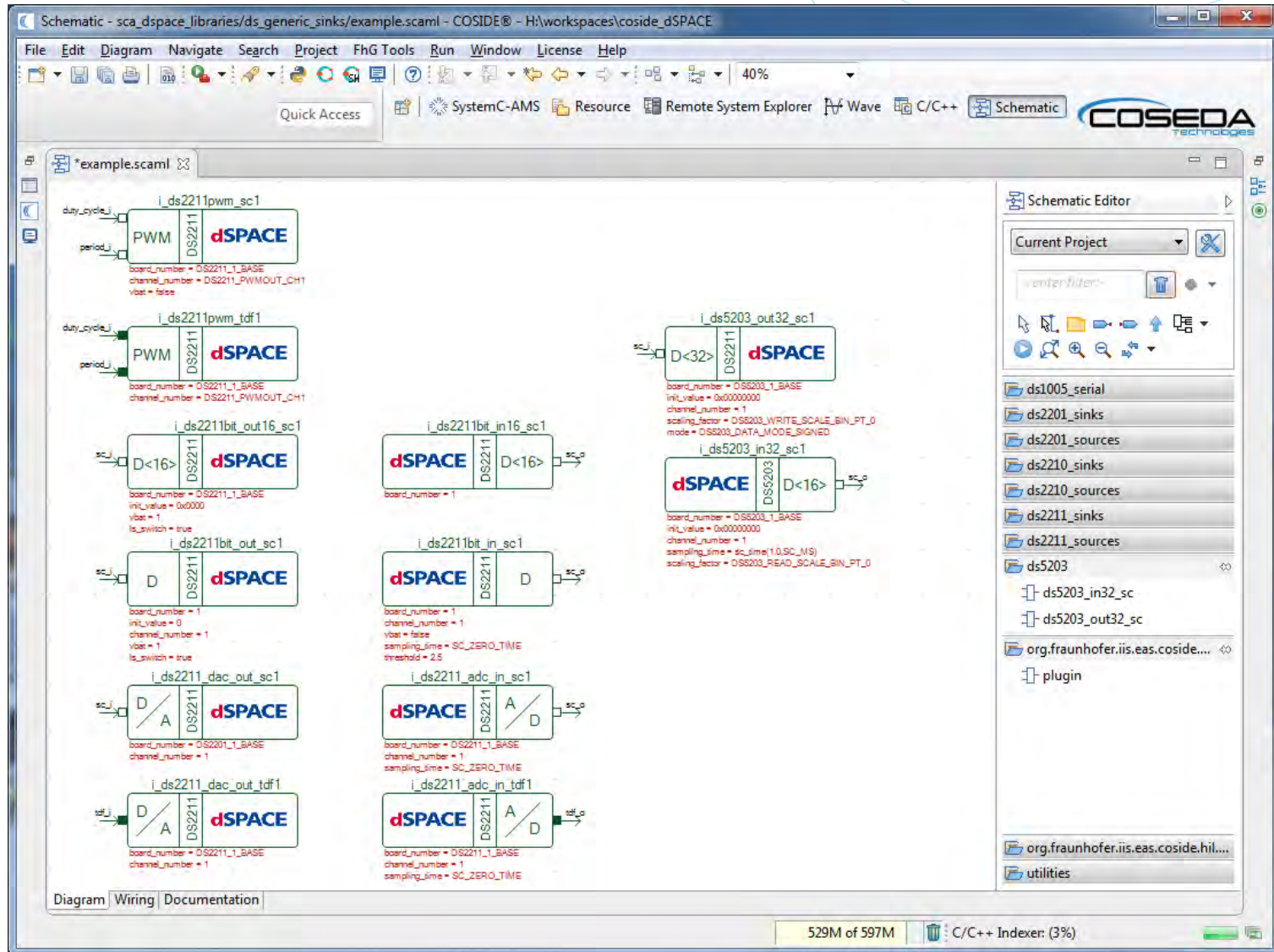


Development Environment



- COSIDE® model entry
- dSPACE specific Menus
- ControlDesk Waveforms & Console

Interface Library



Agenda

1. Introduction
2. Tooling
3. **Failure Injection**
4. Demonstrator

■ Properties

- Non intrusive failure injection, without model changes
 - Failure cases are connected into the netlist dynamically during runtime
 - Thread based for independent de/-activation
- Failure scenario are build up hierarchically
 - Reusability (e.g. failure structures and scenarios)
 - Unified interfaces (for e.g. initialization, de/-activation)
- Error location and time can be scattered statistically
 - Use of extensive statistic library

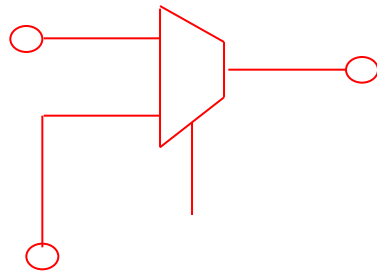
■ Hierarchical test structure

- Testbench
- Testcase/Stimuli without failure injection ← includes additional fault stimuli

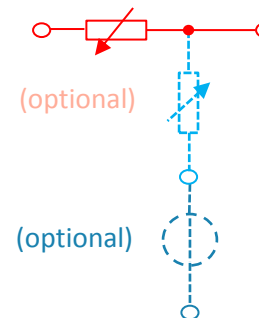
■ Extended hierarchical test structure with failure injection

- Failure stimuli (describes location and time behavior)
- Fault scenario – combination of Fault models e.g. SPI
- Fault models – e.g. Stuck at, Open-Short, Cross Talk ...
- Low-Level-Fault models (e.g. SC/TDF: MUX, ELN: resistor...)

For sc/ tdf connections



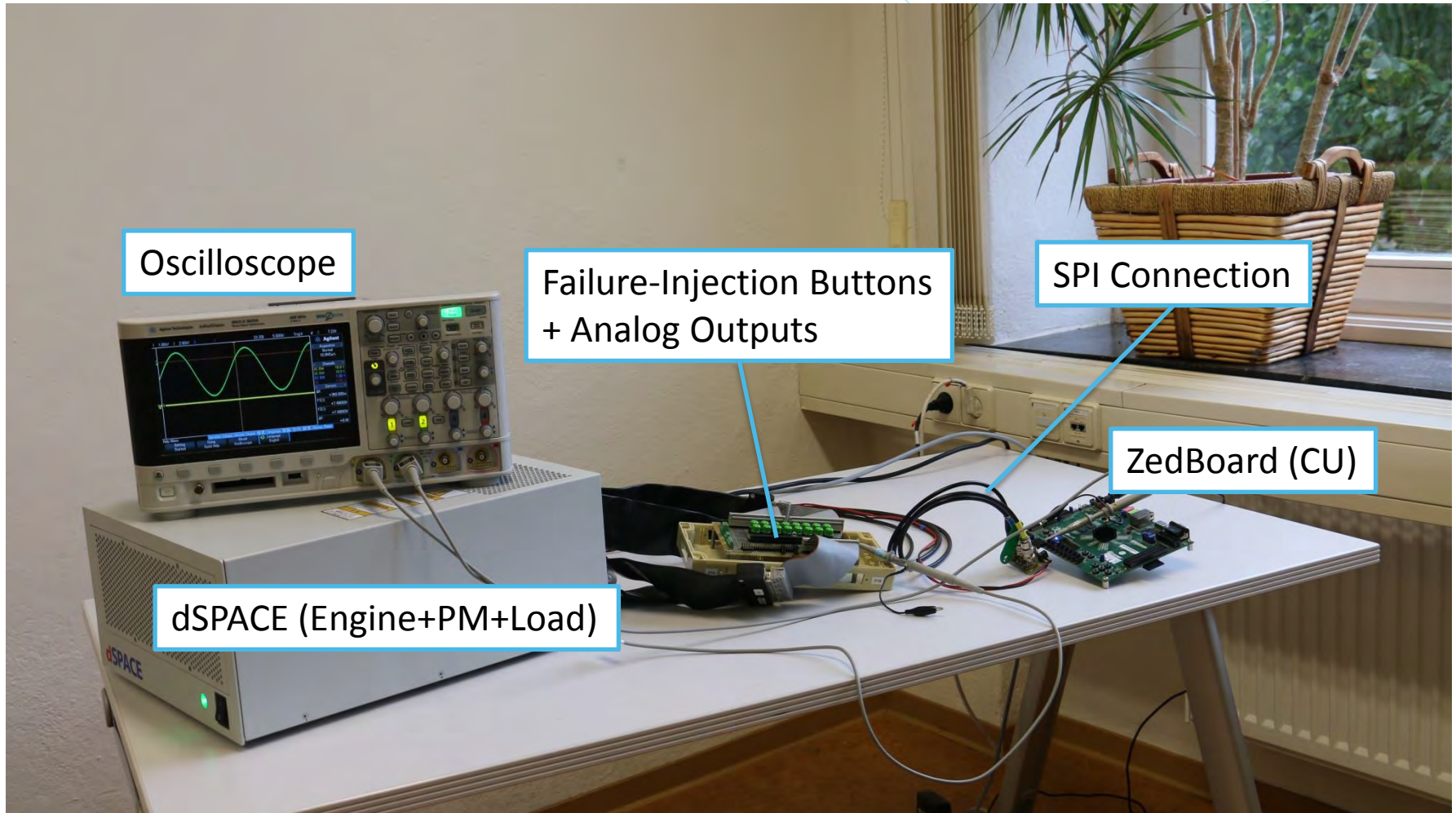
for ELN networks



Agenda

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4. **Demonstrator**

Prototyp Demonstrator

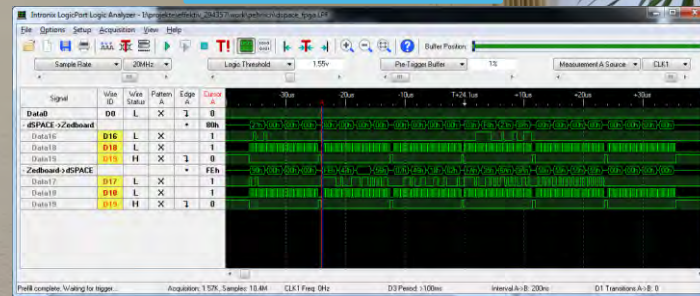


Debug interfaces

Logic analyzer

UART Console

ControllDesk (with console and signal tracing)



```
COM1 - PUTTY
Reading Input Stream
Reading defined test4
new sim offset defined:6000
cleared FPGA clock
01.4944s Manually updating frequency: 50.4128Hz
01.4944s Manually updating frequency: 52.4422Hz
01.4944s Manually updating frequency: 50.4011Hz
01.4944s Manually updating frequency: 47.8096Hz
01.4944s Manually updating frequency: 45.1341Hz
01.4944s Manually updating frequency: 47.1308Hz
01.4944s Manually updating frequency: 49.7403Hz
01.4944s Manually updating frequency: 52.7463Hz
01.4944s Manually updating frequency: 54.5658Hz
01.4944s Manually updating frequency: 57.4038Hz
01.4944s Manually updating frequency: 60.4948Hz
01.4944s Manually updating frequency: 63.8042Hz
01.4944s Overvoltage on VDD detected:520
01.4944s Overvoltage on VDD detected:520
01.4944s Overvoltage on VDD detected:520
01.4944s Overvoltage on VDD detected:520
01.4944s Overvoltage on VDD detected:520
Simulation done
```

Acknowledgement



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■ Thank you for your attention!



 **Fraunhofer**
IIS

SYSTEM C
AMS



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