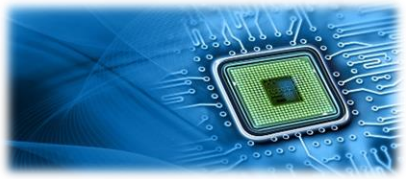
COSEDA® Hardware in the Loop Simulation

Zynq-7000 arm based HIL

COSEDA usergroup meeting 2020

THE ANALOG AND DIGITAL SYSTEM LEVEL COMPANY





COSEDA® Hardware in the Loop Simulation

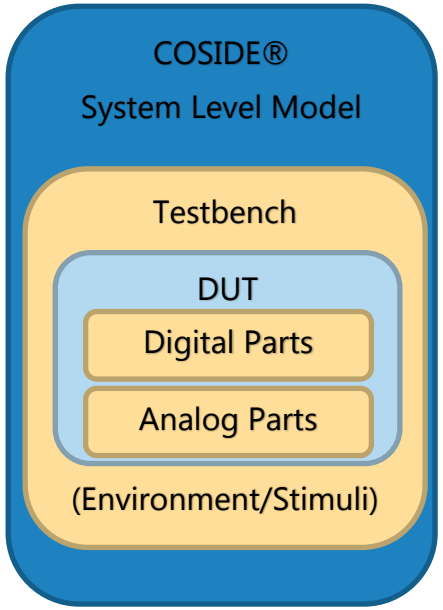
Outline

- Introduction/Motivation
- Flow
- Example platform ZedBoard
- COSIDE integration
- Conclusion/ Outlook

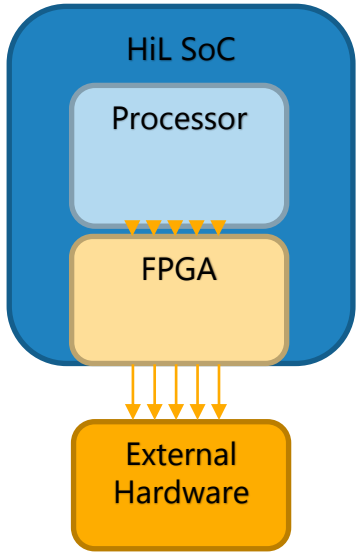
COSEDA® Hardware in the Loop Simulation

Introduction

- System level design
  - SystemC, SystemC AMS, UVM, VHDL/Verilog



- Hardware in the Loop HiL
  - Processor, FPGA, connectivity to External Hardware

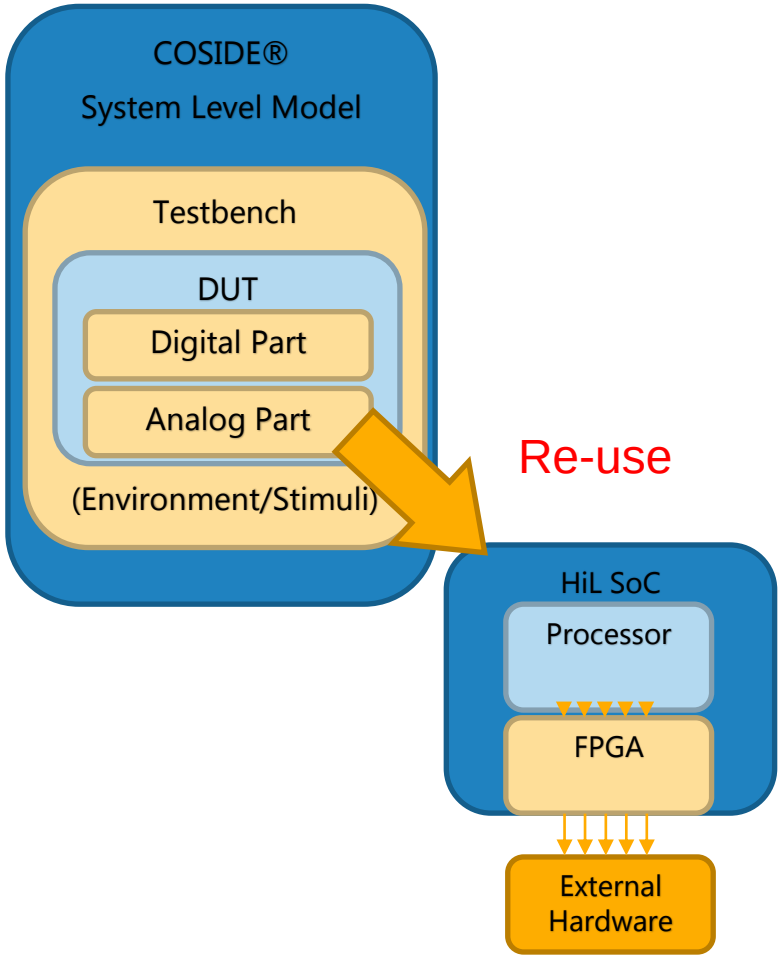


  - Used to test and develop complex real-time embedded systems

COSEDA® Hardware in the Loop Simulation

Motivation

- Re-use / simulate COSIDE® system models/testbenches in a lab environment
- Re-use as much as possible from the COSIDE system level model:
  - **Stimuli** no need to re-write, for real hardware lab validation
  - modeled **Environment** of complex systems (e.g. processor with firmware)
  - **Analog Part** before analog test chips are available, very low hardware costs
  - **Digital Part** as FPGA prototype
- Substitute parts of the model by real hardware / FPGA (sign-off or simulation speed-up)



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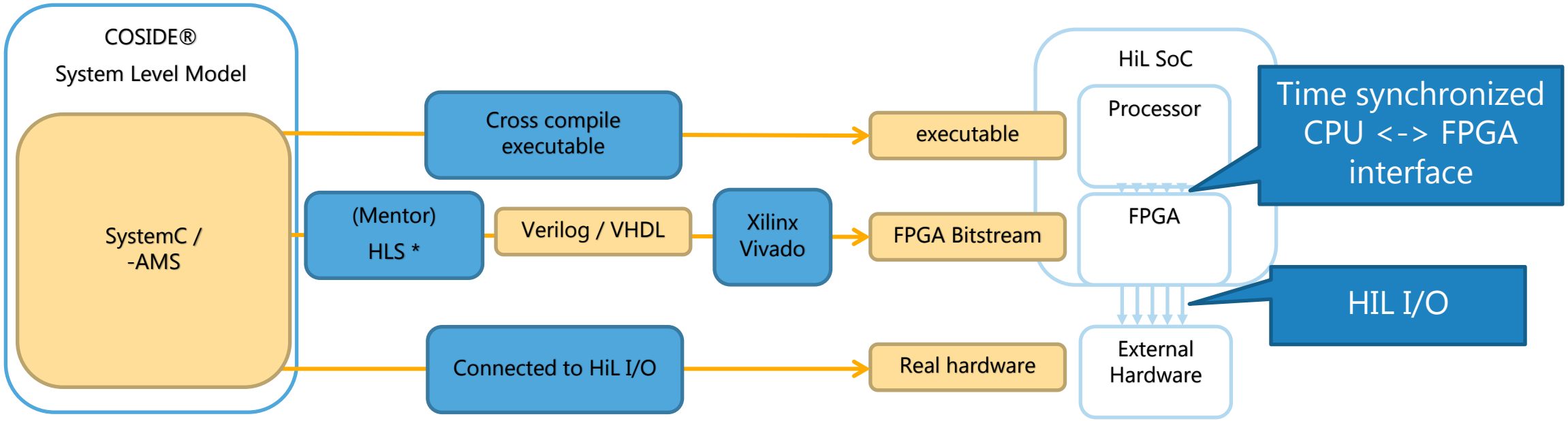
Flow – From COSIDE® System Level Model towards Hardware in the Loop - Example Partitioning

- SystemC / -AMS model has to be mapped to either processor, FPGA or into external hardware
- Steps from the System Level Model towards the HiL simulation:



*if Verilog/VHDL implementation is available this can be skipped

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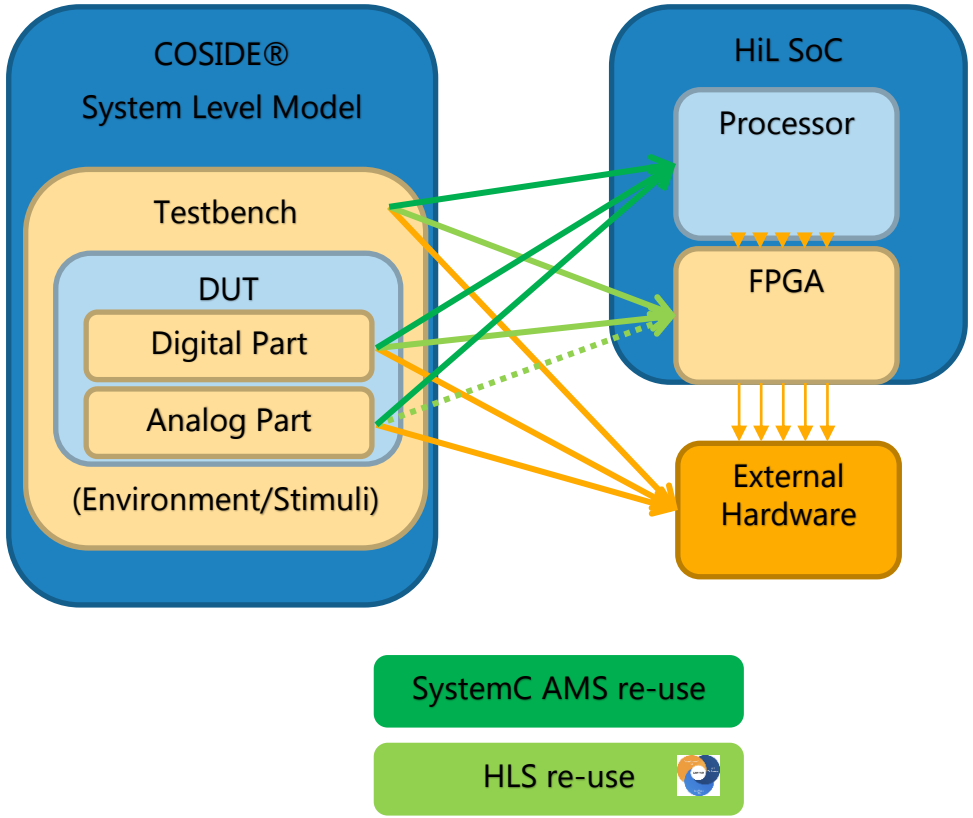
Conclusion

- SystemC / AMS parts are re-used on the processor
- HLS can be used to convert SystemC into synthesizable Verilog/VHDL (even analog parts can be modeled as digital filters)
- Constraints for this partitioning: processor speed, FPGA size, I/O-count, CPU<->FPGA interface (timing and bandwidth)



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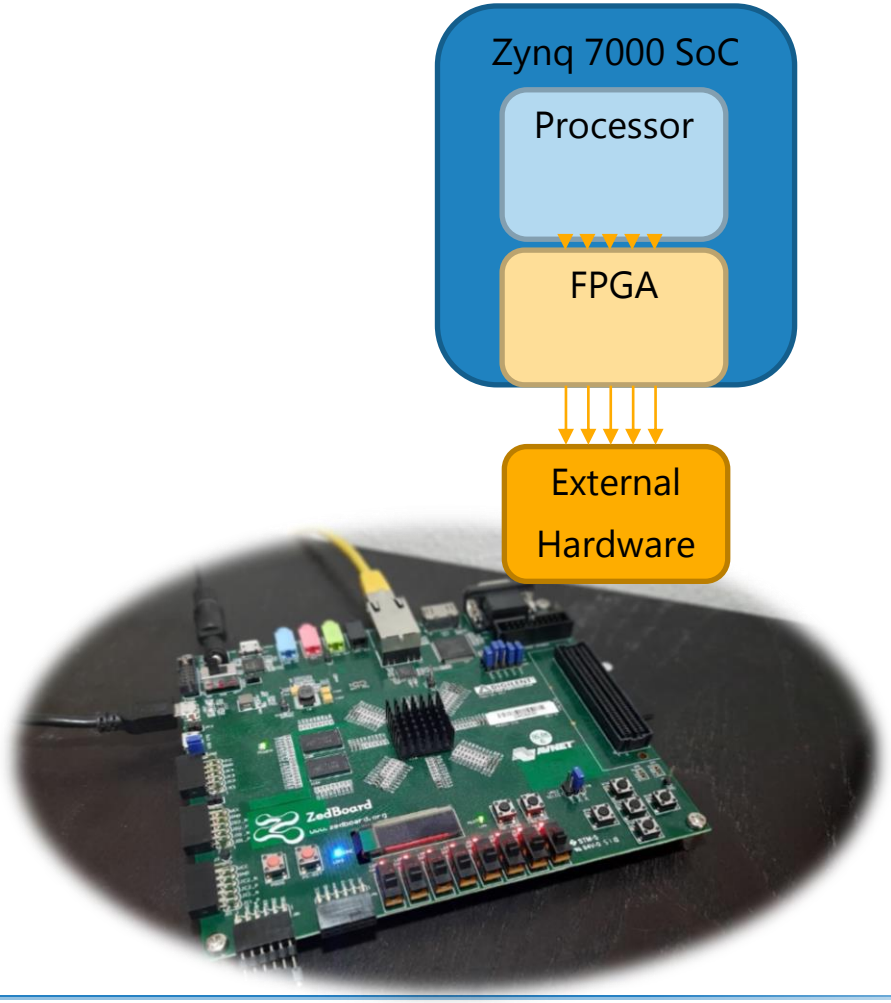
ZedBoard - Example of the Zynq-7000 family

- ZedBoard System on Chip (SoC)
  - 2x A9 ARM cores 666 MHz and 512 MB DDR3 RAM
    - Neon floating point unit
    - Ethernet and SD-Card
  - Programable logic with 85k logic cells (FPGA)
  - Fast interconnect between processor and FPGA
  - 100+ I/O's to external hardware including FMC, buttons, LEDs …



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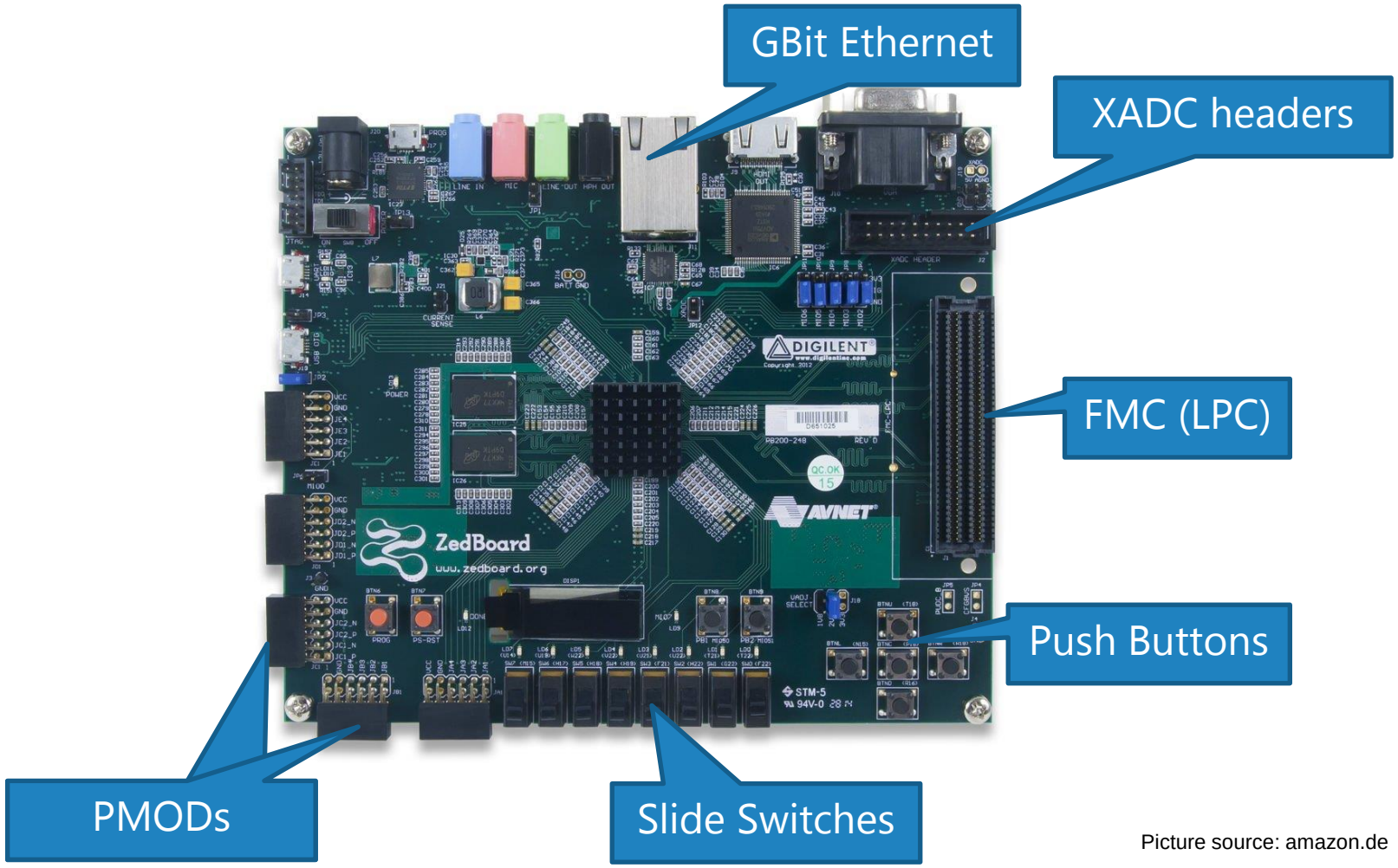
ZedBoard - I/O



Picture source: amazon.de

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COSIDE integration - ZedBoard Pack

- COSEDA provides a ZedBoard pack
  - Real-time patched Linux system
  - GCC cross compiler with hard float neon support
  - SystemC with ARMv7 Quick Thread patch and SystemC AMS
  - Full COSIDE® library stack 800+ elements cross compiled for ARMv7

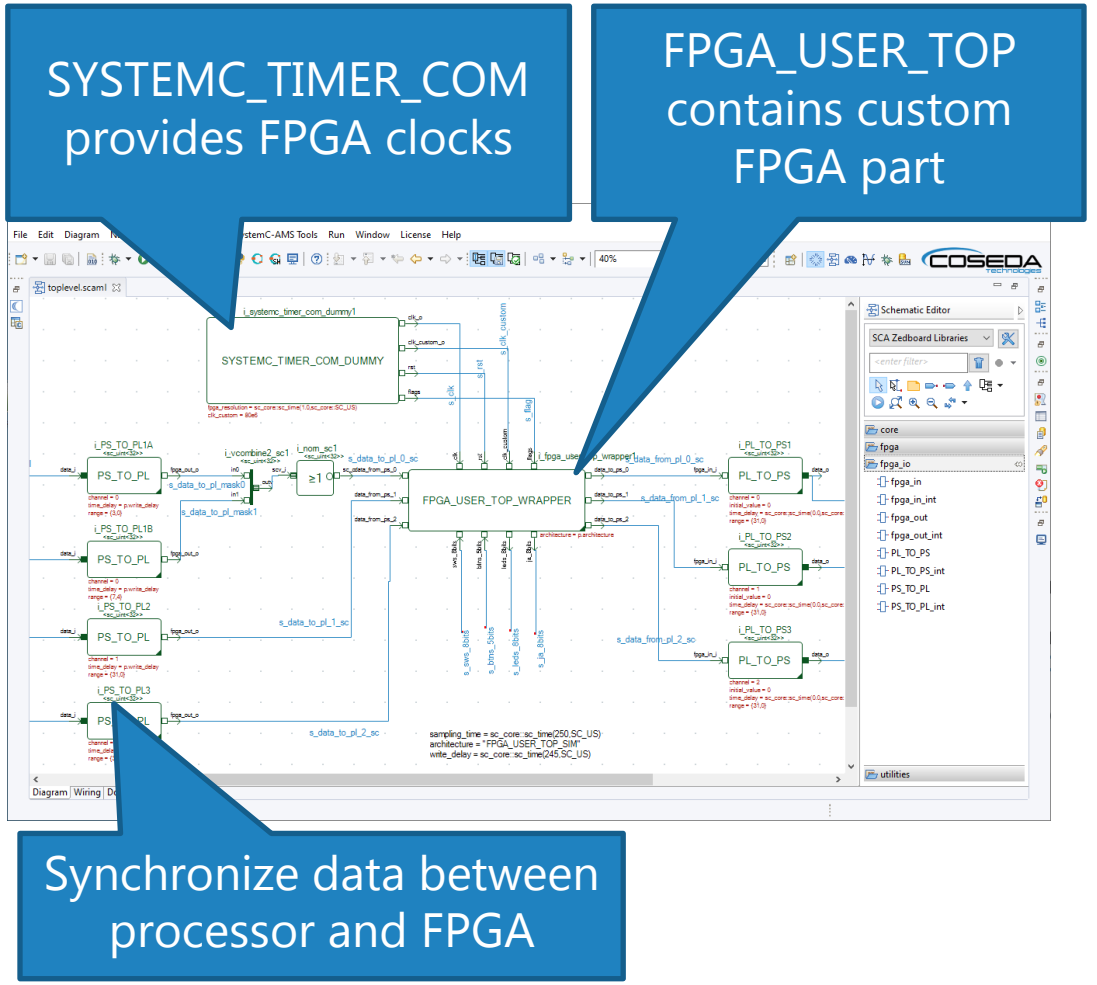
SYSTEMC™

SystemC AMS
PROOF OF CONCEPT 2.3

COSEDA® Hardware in the Loop Simulation

COSIDE integration - schematic

- Graphical partitioning within COSIDE®
  - Sync modules couple between CPU(PS) and FPGA(PL)
    - For data and time synchronization
  - FPGA_USER_TOP contains the part which will be in the FPGA bitstream
    - High level synthesis can be used
  - SYSTEMC_TIMER_COM_DUMMY
    - Provides FPGA clocks to the SystemC model



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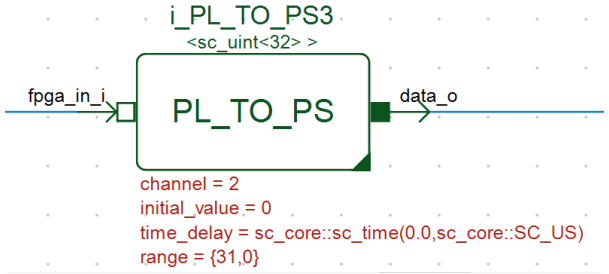
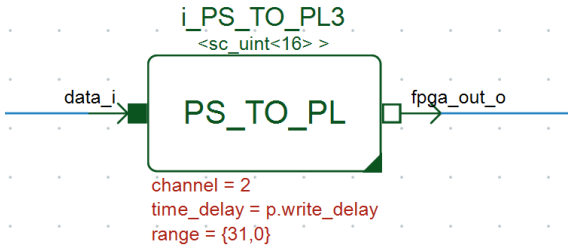
COSIDE integration - CPU (PS) and FPGA(PL) Interface (sync modules)

- Highly accurate time synchronization mechanism between the processing system PS (CPU) and programable logic PL (FPGA)
  - PL_TO_PS uses a FPGA clock to capture data at a precise point in time
  - PS_TO_PL uses the same clock to write the data at a precise points in time
- Interface consists of 8 channels each 32 bit wide
  - Both direction can handle template types castable to a 32bit integer
  - The range attribute allows the combination of smaller signals into an 32bit integer





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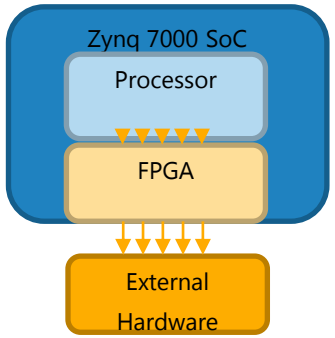
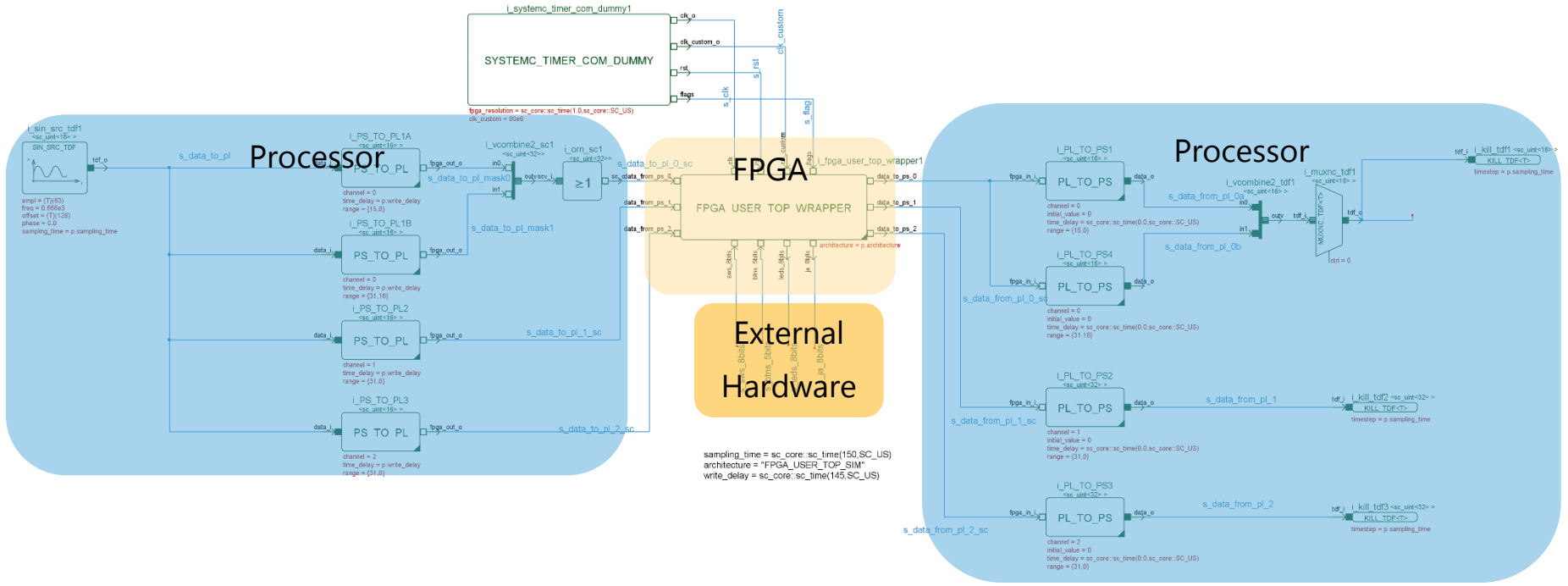
COSIDE integration - Partitioning





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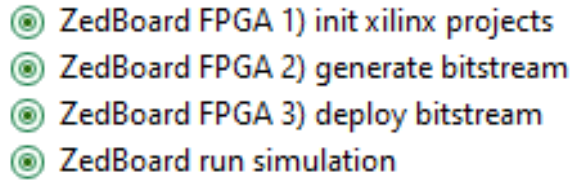
COSIDE integration - Vivado Tool integration

- COSIDE manages Xilinx flow including the bitstream generation via build targets
  - COSIDE manages the Xilinx environment
    - generates Block Level IP of the users Verilog part
    - Includes a coupling IP for timing and data synchronization
    - Manages the constraints file to describe interface to external hardware
  - COSIDE allows bitstream generation and live deployment to the ZedBoard



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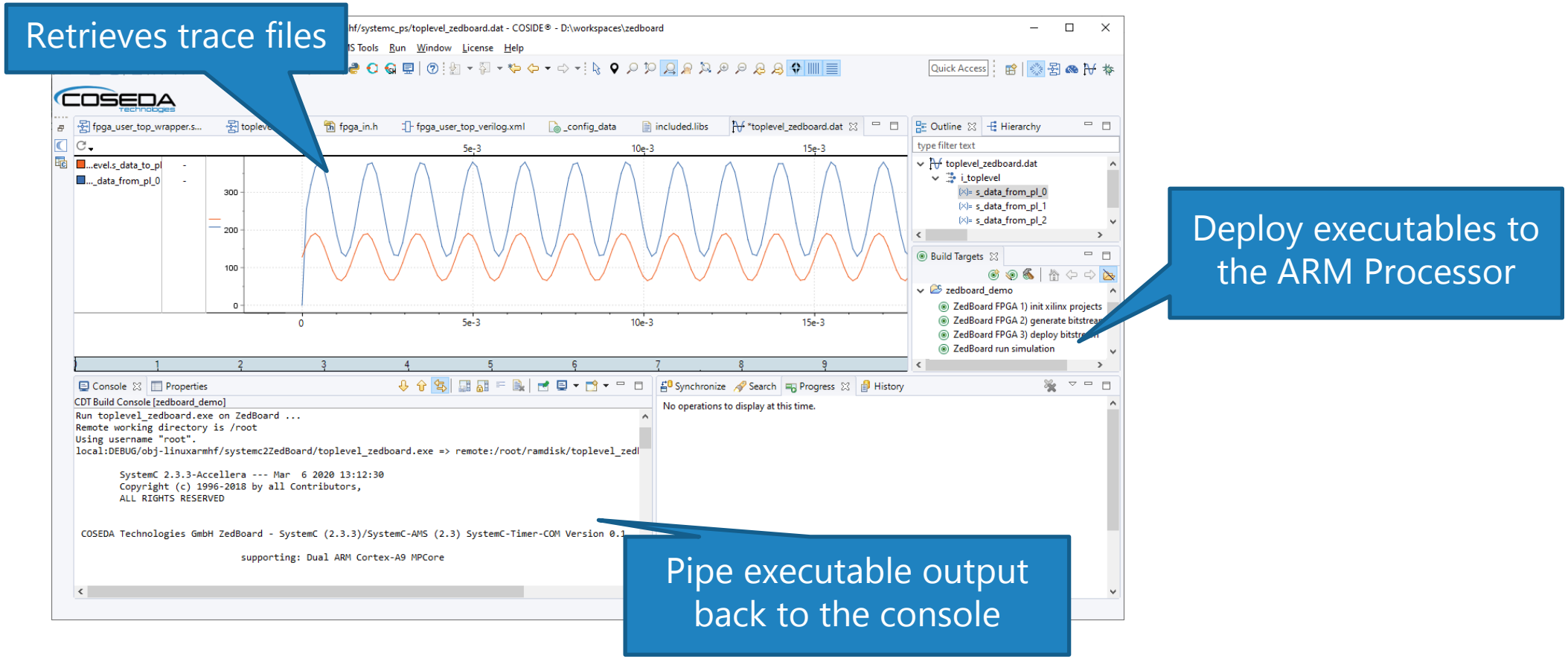
COSIDE integration - simulation control frontend



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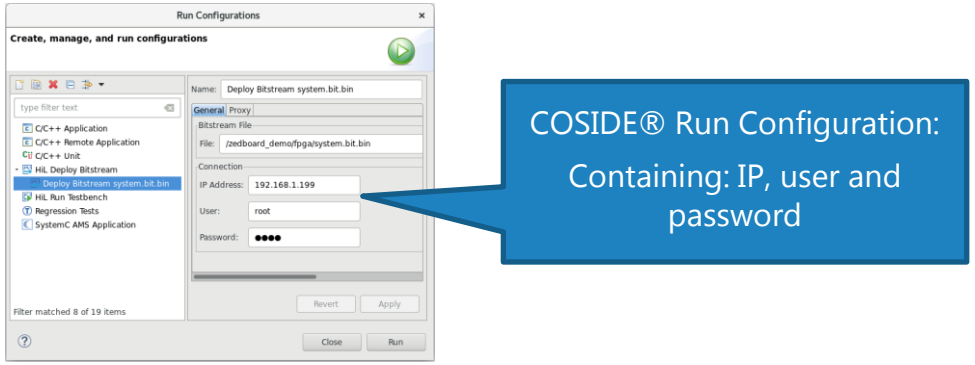
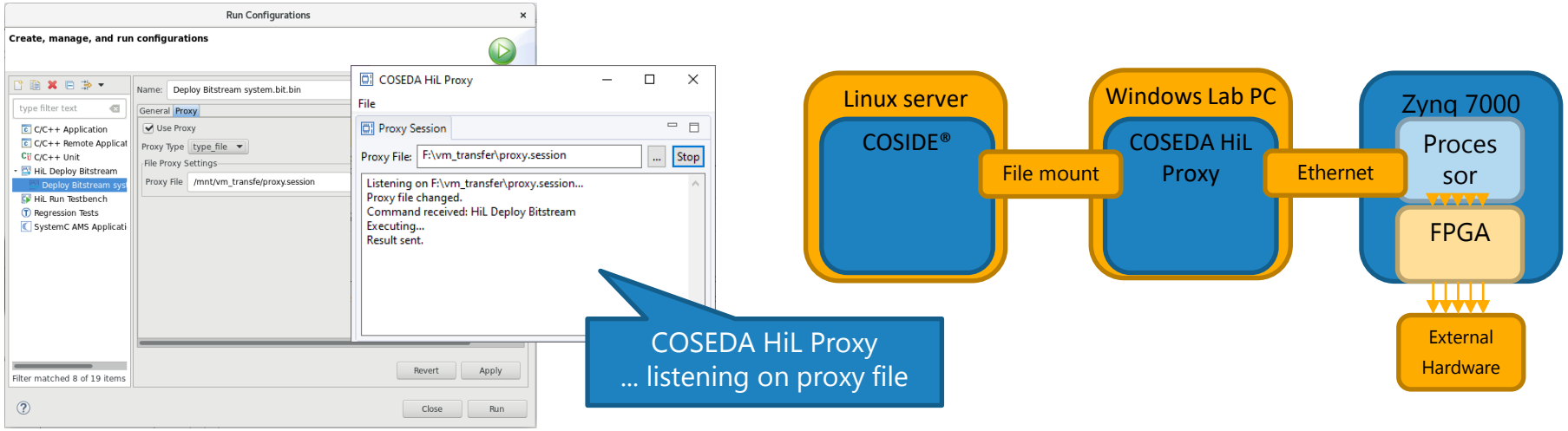
COSIDE integration - ZedBoard communication

- Normal communication via Ethernet



- The COSEDA Proxy allows to control the ZedBoard from a Linux server via a shared file



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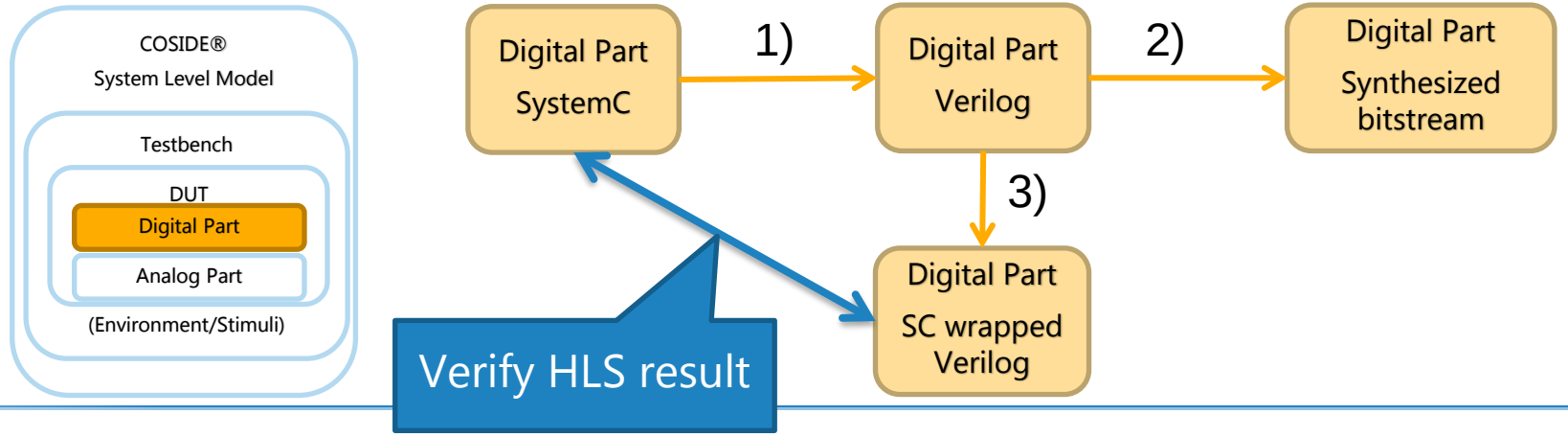
COSIDE integration - Extension: Verilog Co-simulation & HLS

- 1) High level synthesis HLS to replace selected SystemC- by (System-)Verilog-(AMS) modules (e.g. Mentor Catapult)
- 2) Synthesized Verilog to FPGA bitstream
- 3) Simulator coupling to wrap Verilog into the SystemC simulation (e.g. Cadence Incisive, Xilinx xsim, Verilator)



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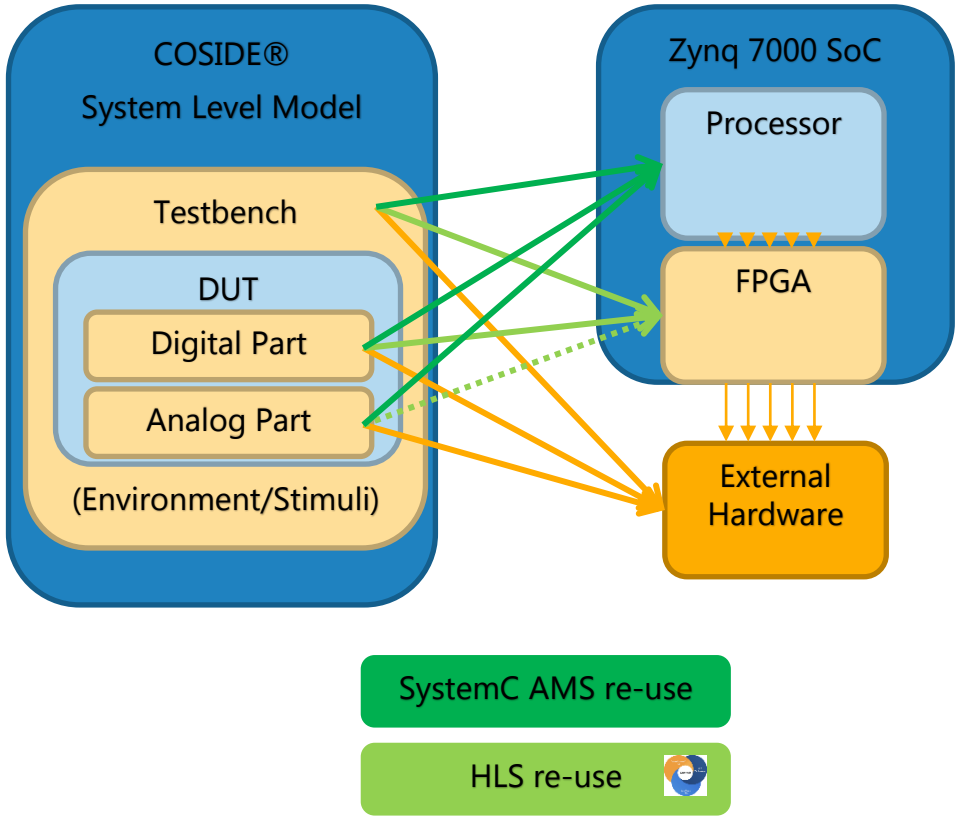
Conclusion

- All models parts are mapped into either CPU, FPGA or into external hardware
- Partitioning is done on schematic level
- COSIDE supports Mentor HLS and Vivado bitstream generation
- COSIDE provides as Addon ZedBoard pack with cross-compiler, sync modules and libraries
- HiL simulation is controlled from within COSIDE®



Outlook

- Outlook
  - Further flow improvements … adoptions towards other boards
  - Analog synthesis into FPGA as digital filters models
  - Looking forward for challenges and new projects in this area

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Thank you for Your Attention

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