System Level Simulation of a Gigabit Radio Transmission System

Ralf Kakerow*, Uwe Knöchel**, Uwe Eichler**, Erwin Hemming*

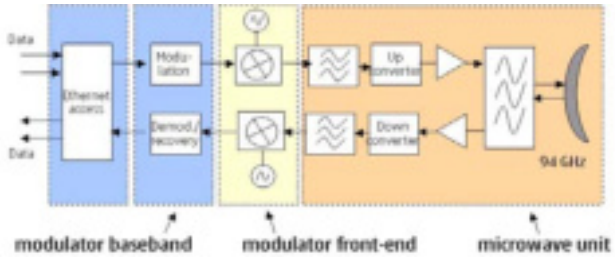
* Nokia Research Center,
Bochum, Germany
ralf.kakerow@nokia.com

** Fraunhofer Inst. for Integrated Circuits (IIS),
Branch Lab Design Automation (EAS), Dresden, Germany
knoechel@eas.iis.fraunhofer.de

Introduction. The Gigabit Radio transmission system is a point-to-point radio link that addresses the connection of hotspots and last mile end points to a gigabit infrastructure. Digital modulation techniques provide high spectral efficiency and scalable data rates. The system transmits in the E-band at frequencies up to 90 GHz. A maximum data rate of 1250 Mbps can be reached.

The design of such a system is a multi-disciplinary task that covers RF and microwave technology, digital signal processing and understanding of Gigabit-Ethernet [1]. The complexity of the system, the high data rate and different time constants in the subsystems (carrier and intermediate frequency in the GHz domain and timing recovery at kHz) require a high efficiency of the system level simulation, which is achieved by using static dataflow simulation and complex baseband modeling of the RF and microwave parts [5]. Thereby two main tasks have to be solved: how to model timing variations in static dataflow and how to describe the behavior of RF frontends in complex baseband.

System architecture. The system consists of four main modules: Ethernet access, digital baseband modem with π/4 DQPSK modulation, modulator IF frontend that converts the signal to/from the 3 GHz intermediate frequency and the microwave unit for the conversion to the carrier frequency in E-band.



Gigabit Radio System Architecture

An essential part of the receiver subsystem is the symbol timing recovery. It determines the optimum sampling point for the received signal, which is a precondition to detect the transmitted information. The high signal bandwidth requires a very efficient implementation of DSP algorithms used for this task. Due to the limited signal processing performance of the FPGA-based prototype, the transmitted signal is over-sampled by factor two only. Therefore a mixed-signal timing recovery loop was implemented, where the digital part controls the sampling oscillator that triggers the A/D converters to catch the optimum sampling point. The early-late algorithm is used in the digital eye diagram detection module to compute the timing error [4].

Simulation concept. Using C/C++ for system-level modeling provides several advantages: flexibility in description of the abstracted algorithms, fast code execution, compatibility with many simulation tools and nearly all platforms, reusability for DSP programming. A disadvantage is the rare support by integrated simulation tools so that custom solutions are needed for testbenches, postprocessing and visualization in most cases.

As a practical solution the SystemC-AMS library was used to implement the Gigabit Radio system model. It extends the capabilities of SystemC in the area of dataflow and mixed-signal simulation. Also an Eclipse-based simulation environment with schematic entry and waveform viewer is available[6].

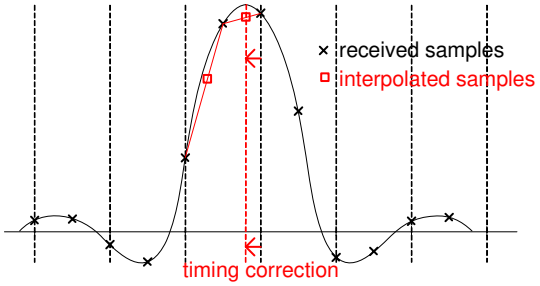
Jitter modeling in dataflow simulation. From a system-level point of view analog-to-digital conversion is mainly sampling of the time-continuous signal. However, when using dataflow modeling, time is already discrete, also for the analog blocks. The most obvious solution – oversampling of the analog signal by a factor of n – is not really a solution because n has to be chosen fairly large in order to simulate even small variations of the sampling point and would then neglect the performance advantages of system simulation.

To overcome this problem, a sampling block with interpolation has been implemented. A shifting of the sampling points in time as requested by the timing recovery block is not possible in the dataflow domain with its fixed time steps. Instead, a signal value between two successive sampling points is interpolated according to the requested time shift. The main advantage of this approach is that the number of samples is maintained as required by the dataflow principle. The arising timing error is reasonable since in the real system the digital baseband part works with the sampled data as if they were equidistant.

So far linear interpolation is used. Experiments using a windowed sinc interpolation show slightly better results. The introduced modeling error is justified for system-level simulation where fast simulation is required to get estimations for overall performance measures like bit error rates.

The presented work was partly supported by the German BMBF within the research project DETAILS (01M3071).

Changing sample times using interpolation also allows jitter modeling. Statistical changes in the sampling time are referred to as jitter and occur due to noise processes in oscillators. In the system-level model jitter is added as a phase noise source with Lorentzian spectrum [7] to the phase offset signal from the timing recovery to the sampler block. This reflects timing jitter of the sampling oscillator as well as phase noise of the demodulator in the receiver frontend.



Timing correction by interpolation

RF frontend models. The RF subsystems have an important impact on the overall system performance. Crucial signal deviations that can occur in the RF frontends comprise quadrature, bias and balance errors. Without digital compensation, these errors will cause an increased bit error rate (BER) and may disturb the symbol timing recovery. Concerning the carrier frequency at about 90 GHz and an intermediate frequency at 3 GHz, modeling in the complex baseband domain [2][3] is a must. Two different kinds of models are used.

In top-down design, for an early exploration of the system performance fast models of RF imperfections at a high level of abstraction are used. The mentioned three kinds of distortions are applied to the complex baseband signal in two different SystemC-AMS modules in the following manner: quadrature error: `I_out = I_in; Q_out = I_in * sin(quad_err) + Q_in * cos(quad_err);` bias and balance error: `I_out = biasI + balanceI * I_in; Q_out = biasQ + balanceQ * Q_in;` To enable a test of the compensation algorithms, random values of the errors are selected from a specified range at the initialization of the simulation.

The behavior of dedicated frontend architectures is more complicated, because it depends on the properties and the matching between the components. RF simulation tools provide the required modeling and simulation capabilities to analyze the separated RF subsystems. The bottom-up generation of table based models allows the validation of RF designs in the system context. The models are created automatically by a characterization of the circuit-level models. The generated tables store complex gain values in dependence on parameters like frequency, power and phase. The system-level model then contains a module that represents the characterized blocks in complex baseband. It reads the generated tables and calculates the complex gain with respect to the actual input frequency, power and phase. These table models need fast interpolation algorithms, which can efficiently be implemented using C/C++.

Simulation results. The system-level simulation comprises transmitter, channel and receiver of the Gigabit Radio. Due to the high abstraction level of the model and efficient use of dataflow modeling a simulation speed is reached that enables the simulation of system behavior like settling of the timing recovery loop and the evaluation of the bit error rate (BER) in consideration of effects like compression, phase noise and other frontend imperfections like quadrature or bias error.

Most of the modeling and simulation tasks were done using the SystemC-AMS development environment which provided easy to use schematic editor, waveform viewer and source code management. Existing algorithms e.g. for interpolation needed in the ADC model and the baseband table models could easily be integrated in the C++ models. It should be noted that the environment and the SystemC-AMS library itself are still under development. A useful extension would be a library of RF building blocks like amplifiers, mixers or filters.

The system concept was successfully proofed also on a hardware prototype.

References

[1] Kakerow, R.: Modelling Technologies for Disruptive Communication System Design. FDL'05, Lausanne, Switzerland, 2005.

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[4] Bergemans, J.: Digital Baseband Transmission and Recording. Kluwer Academic Publishers, Boston 1996

[5] Knöchel, U.; et al.: Analyse eines Gigabit-Funksystems mit AMS Designer. Analog'06 , Dresden, September 2006

[6] SystemC-AMS Homepages: systemc-ams.eas.iis.fraunhofer.de, www.systemc-ams.org

[7] Poore, R.: Phase Noise and Jitter. Agilent Technologies, 2001, http://eesof.tm.agilent.com/pdf/jitter_phasenoise.pdf

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[1]) Nokia Research Center, SRC Bochum
[2]) Fraunhofer Institute for Integrated Circuits (FhG-IIS/EAS)

SystemC-AMS Workhop
26 Jun 2007, Dresden

SPONSORED BY THE
Federal Ministry of Education and Research
BMBF Grant 01M3071

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Overview

- Technology
- Architecture
- IF front-end
- Modulator baseband
- System-level simulation
- Hardware demonstrator
- Results

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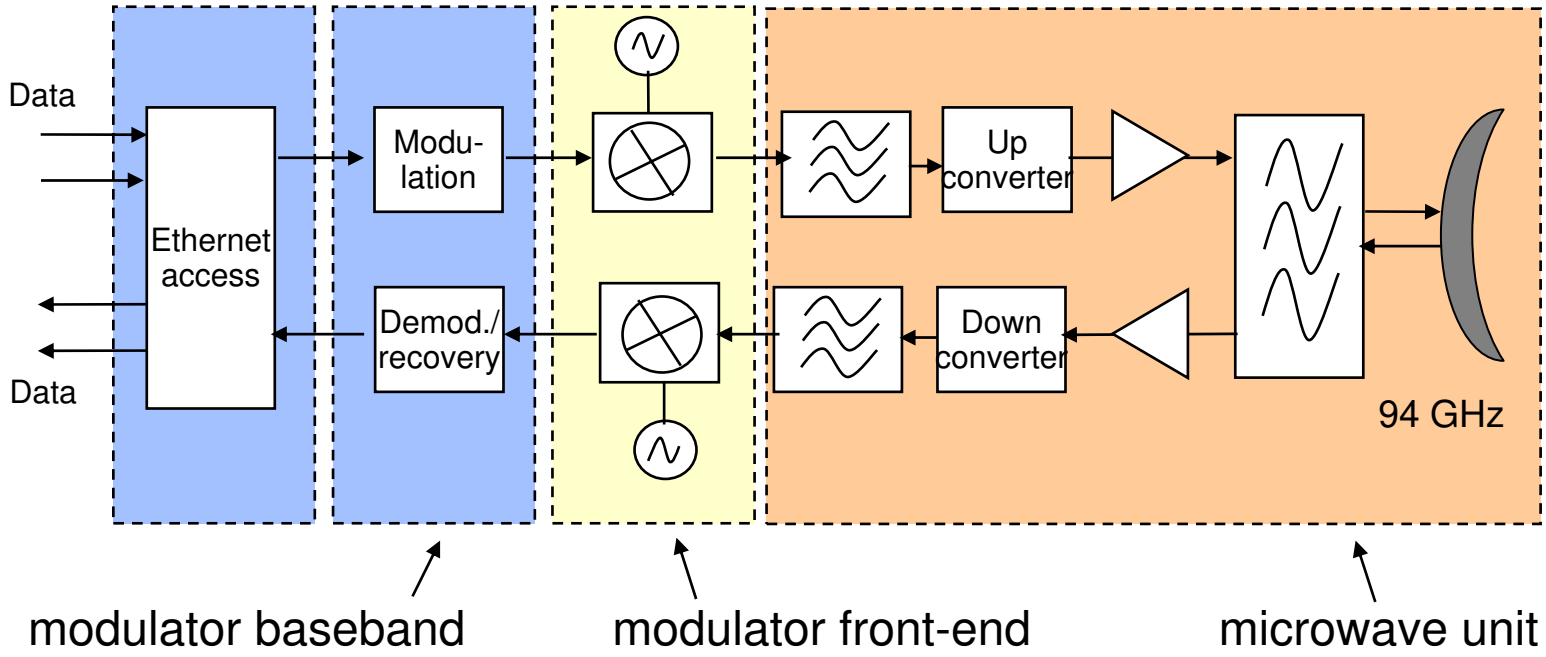
Gigabit radio technology

- Point-to-point Gigabit Ethernet link as cable replacement
- Data rates of 1 Gsps or more with a range of up to several km
- Operation in E-band (specification by FCC and ETSI ongoing)
- Disruptive technology challenging fiber optics
  - short and simple installation, flexible
  - only a fraction of fiber optics cost
- Cost attractive to network provider for “last mile” connection

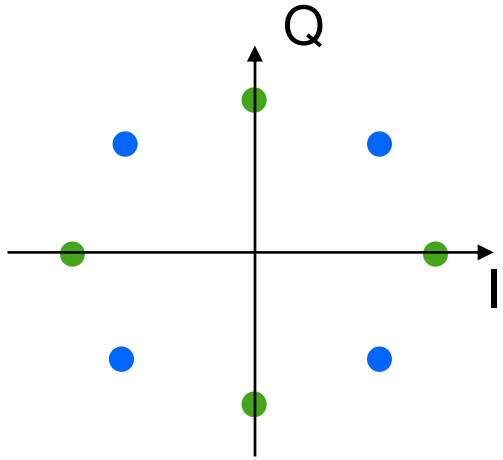
- First players are already on the market with 1 Gbps
  - current systems are based on simple modulation schemes like On-Off Keying (OOK)
  - 3.125 Gbps already on the roadmaps
  - limited frequency ressources available
  - cost optimized technology vs. scalable “future proof” platform

Overall architecture



- Multi-disciplinary system:
  - Gigabit ethernet access
  - Baseband signal processing
  - Modulator front-end
  - Microwave unit

Modulator

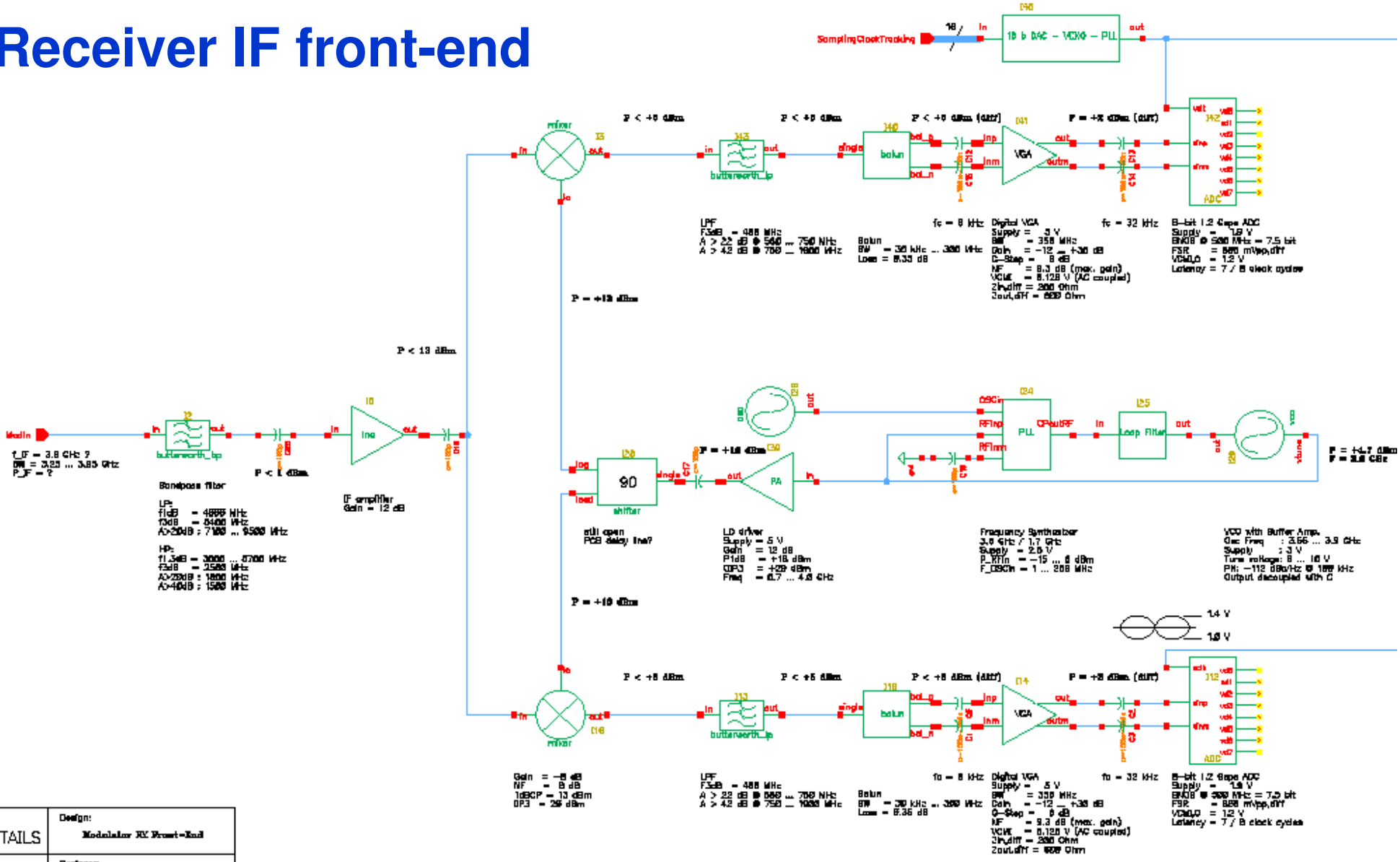


- Operation mode: repeater (for proof of concept)
- Data rate: 1250 MHz
- Modulation scheme: pi/4 D-QPSK
- Modulation bandwidth: 625 MHz
- Spectral bandwidth: around 350 MHz after TX filtering

- I/Q correction: Bias, Balance, Quadrature for TX and RX
- BB/FE regulation loops:
  - ADC sample clock tracking, 16 bit
  - RX IF frequency correction, 16 bit

- Front-end architecture:
  - direct up-conversion to IF
  - microwave LO generation using frequency multipliers
  - TX IF: 3.0 GHz, +13 dBm
  - RX IF: 3.0 GHz, +13 dBm

Receiver IF front-end

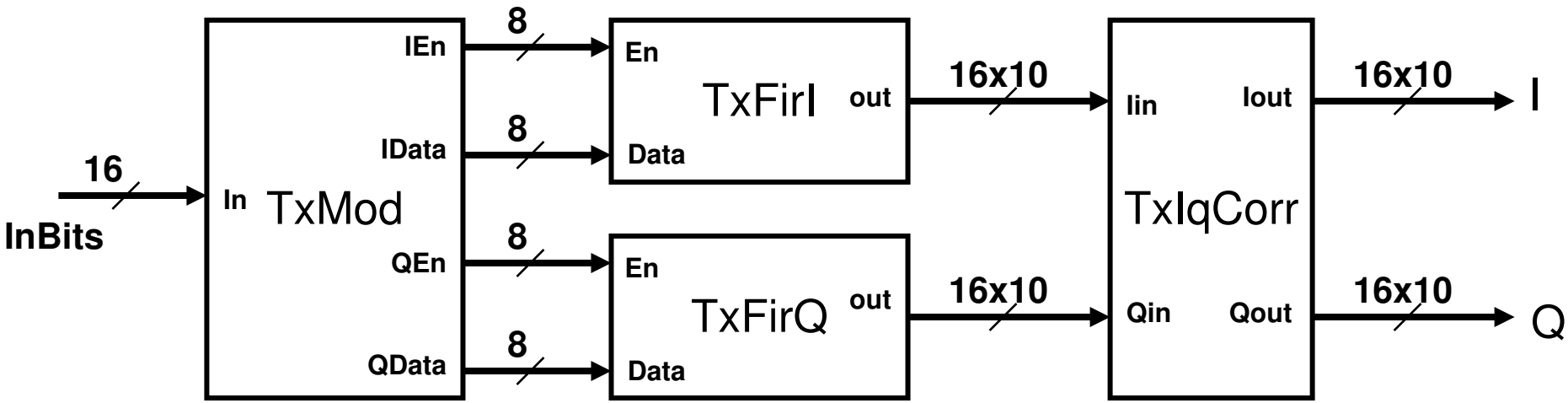


Project: DETAILS	Design: Modulator RX Front-End
Date: 08.10.2004	Designer: Ralf Kakarow

Simplified schematic / behavioural model

Draft version – still under work

Transmitter baseband



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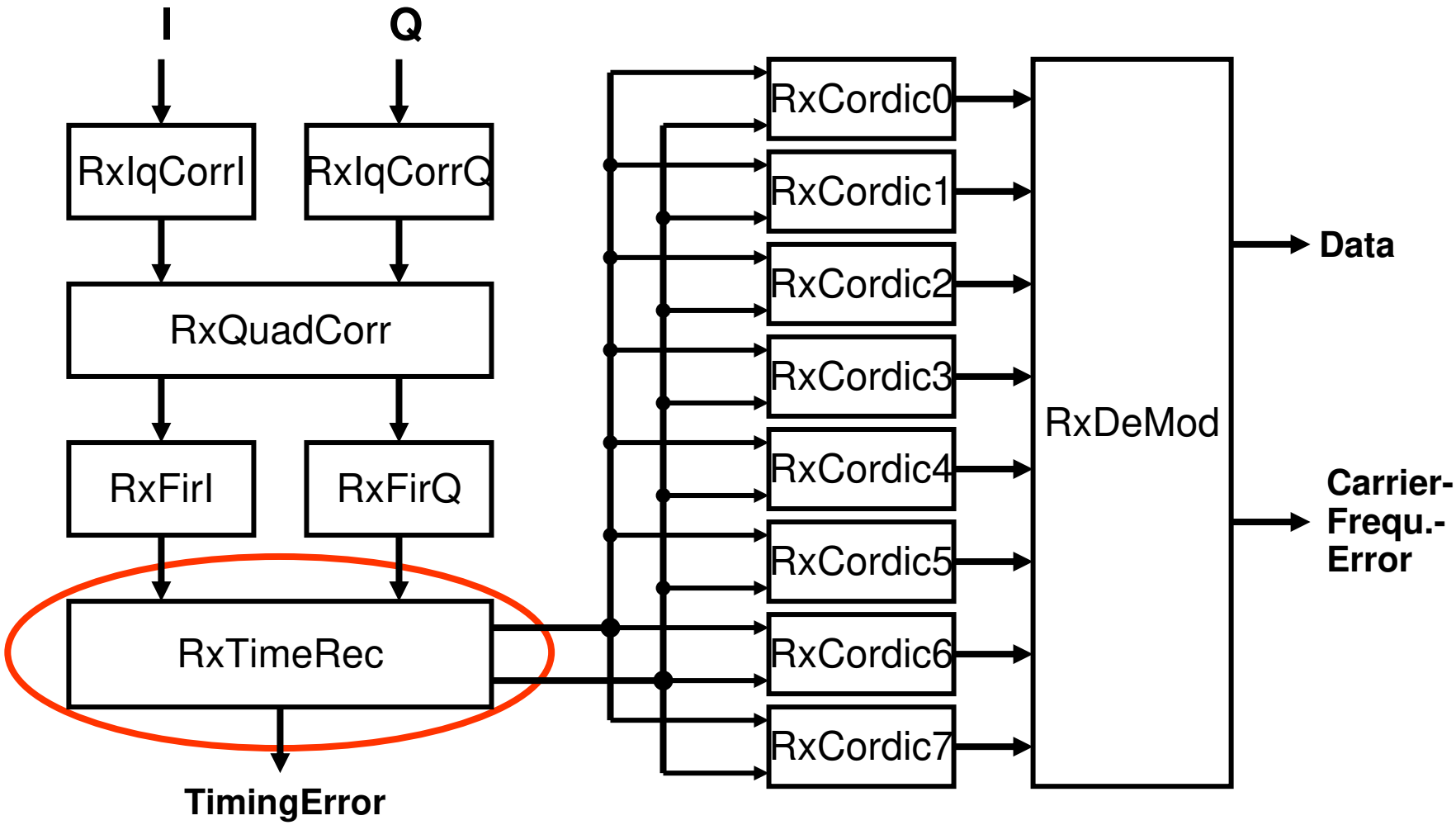
Receiver baseband



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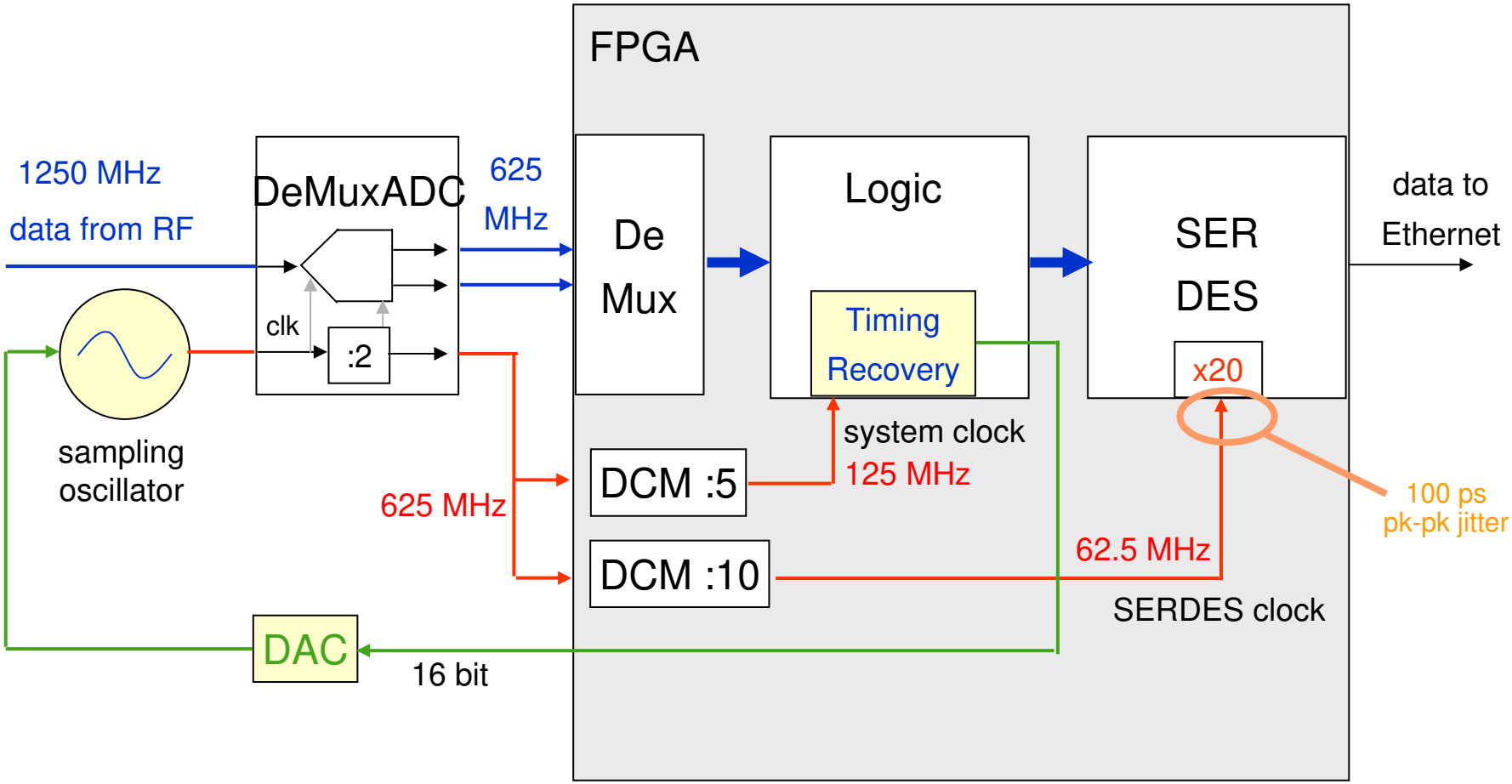
Receiver timing recovery



Modeling challenges

- Raised importance of some parameters when moving to microwave frequencies
  - microwave oscillator phase noise
  - power amplifier linearity
  - receiver gain
  - frequency dependence of components (over signal bandwidth)
  - I/Q errors are always an issue with quadrature modulated radios
- Multidisciplinary system with „specification feedback“
  - tough jitter requirements of Gigabit Ethernet protocol require high clock recovery and distribution performance
- Proto system design performance limited by „off-the-shelf“ components
  - Components usually operate close to or beyond their limits
  - Availability of commercial component models usually quite restricted
- BER simulations
  - “Simple” simulation in SystemC:
    16 billion bits take around 15 hours

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Concept for System Simulation

High simulation efficiency for BER computations

Different timing constants

— static dataflow modeling

— avoiding oversampling

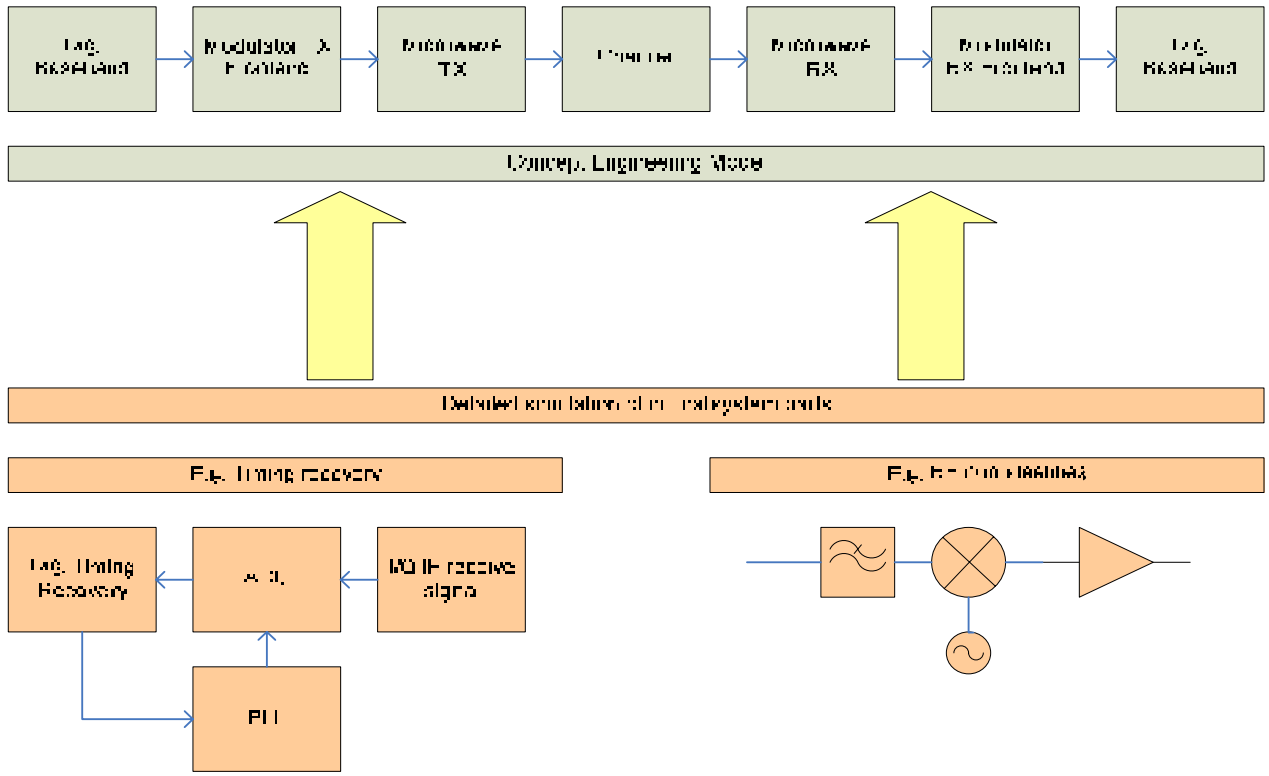
Accurate modeling of critical parts

Settling of timing recovery with respect to jitter

— modeled by interpolation in ADC

Imperfections of analog frontends

— behavioral or table-based in complex baseband



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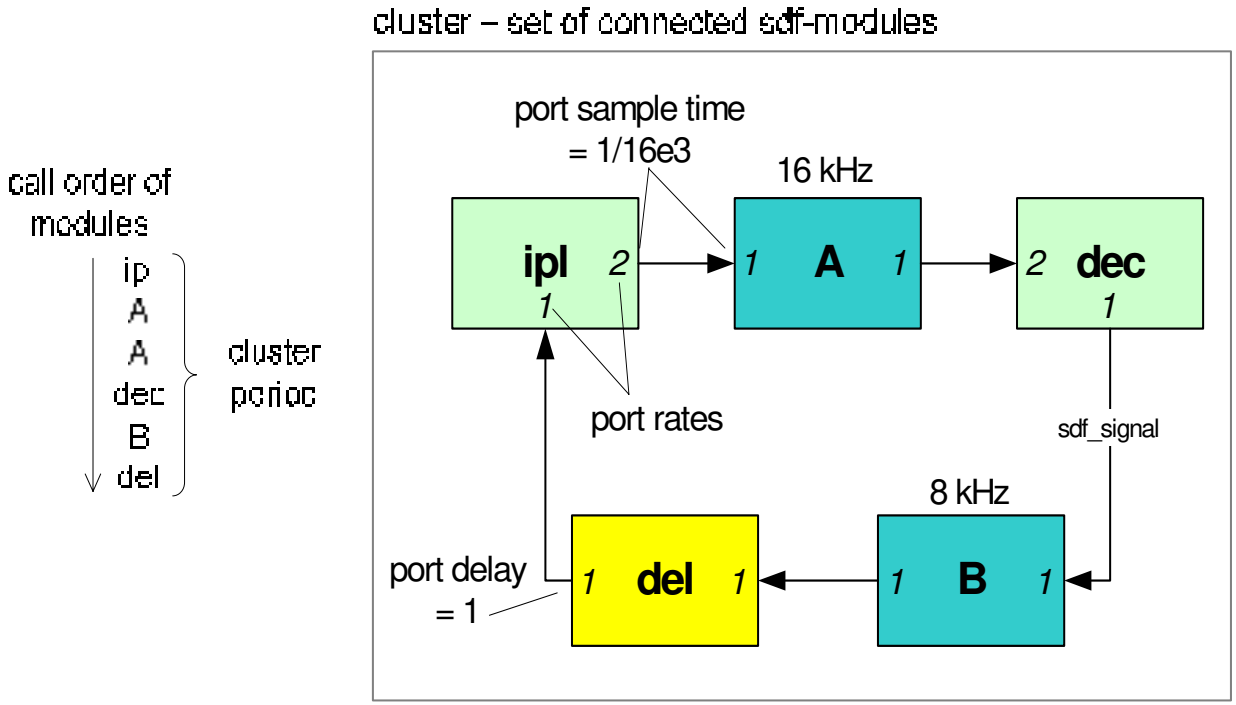
System Level Modeling with static dataflow



— suited for time-discrete systems especial for DSP

— efficient due to scheduling before simulation

— SystemC-AMS was used

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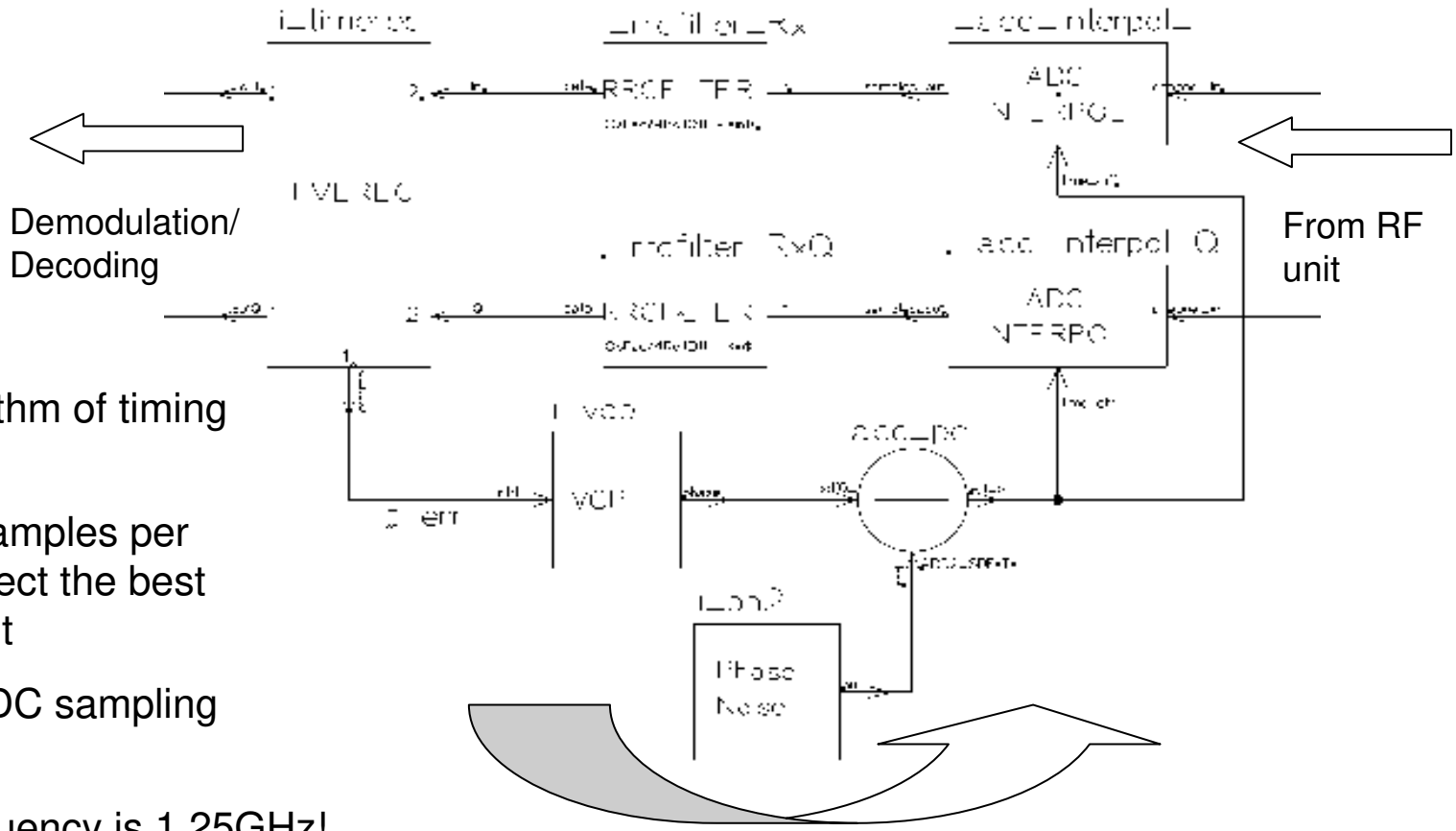
Schematic of Timing Recovery Loop



Early-Late algorithm of timing recovery:

— uses only 2 samples per symbol to detect the best sampling point

— adjusts the ADC sampling point

— sampling frequency is 1.25GHz!

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Timing Recovery – Modeling Challenge

Real System

— continuous time I/Q-signal is sampled with 2 samples/symbol

— timing recovery controls the sampling point

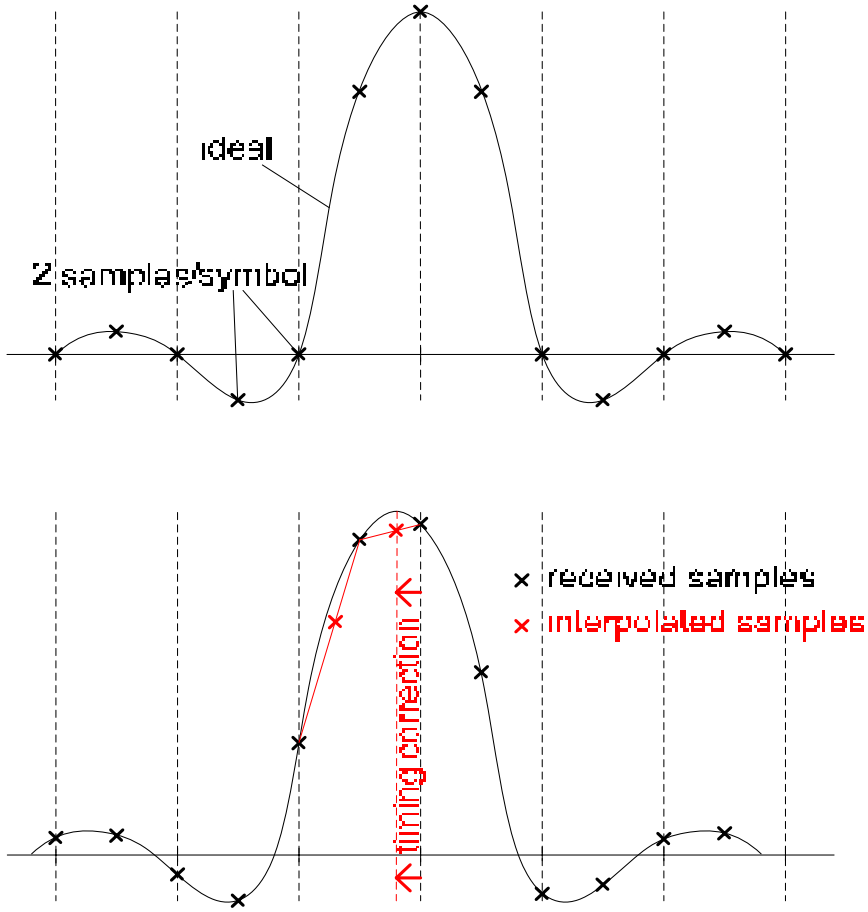
Challenge in Simulation

— avoid additional oversampling of the analog input for performance reasons

Approach

— modified ADC model

— signal values at the corrected sampling points are determined by interpolation



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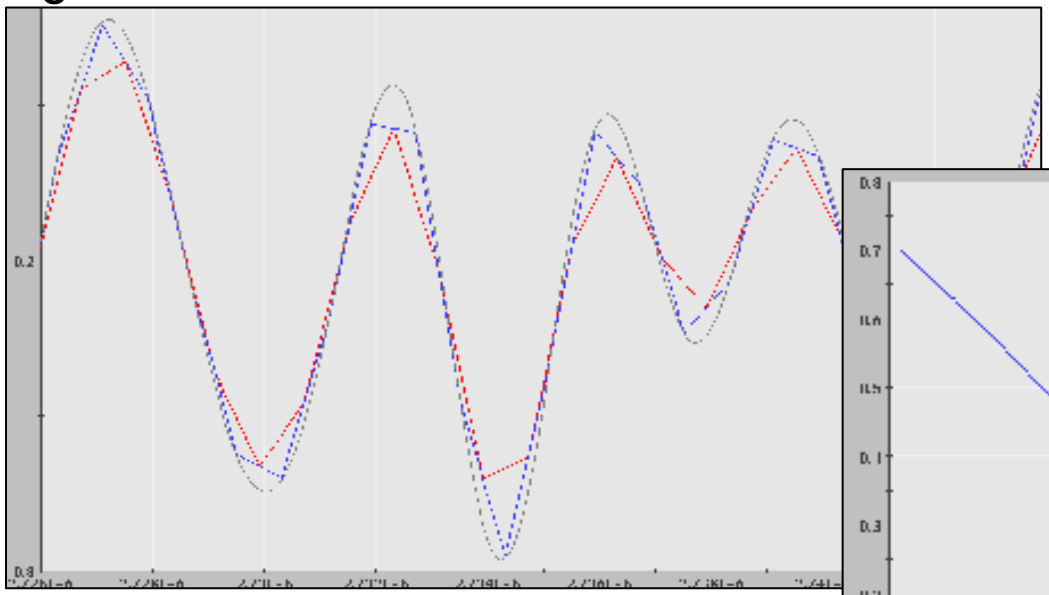
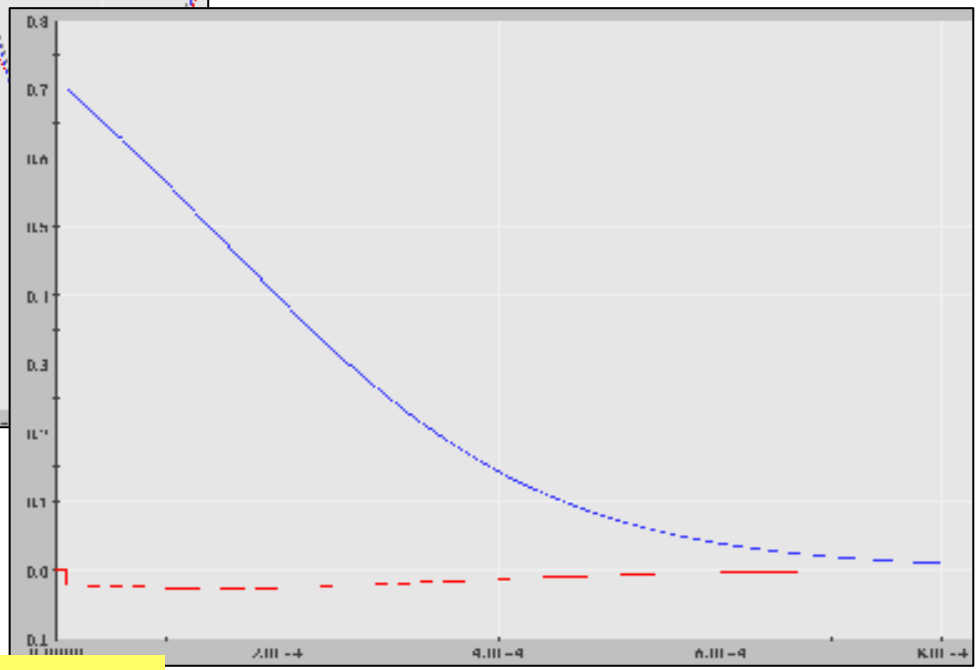
Timing Recovery – Simulation Results

Signals at ADC



analog signal (reality)
sampled signal
after phase correction

Settling



ADC-modeling algorithm effects amplitude error, but fortunately QPSK is robust against this.

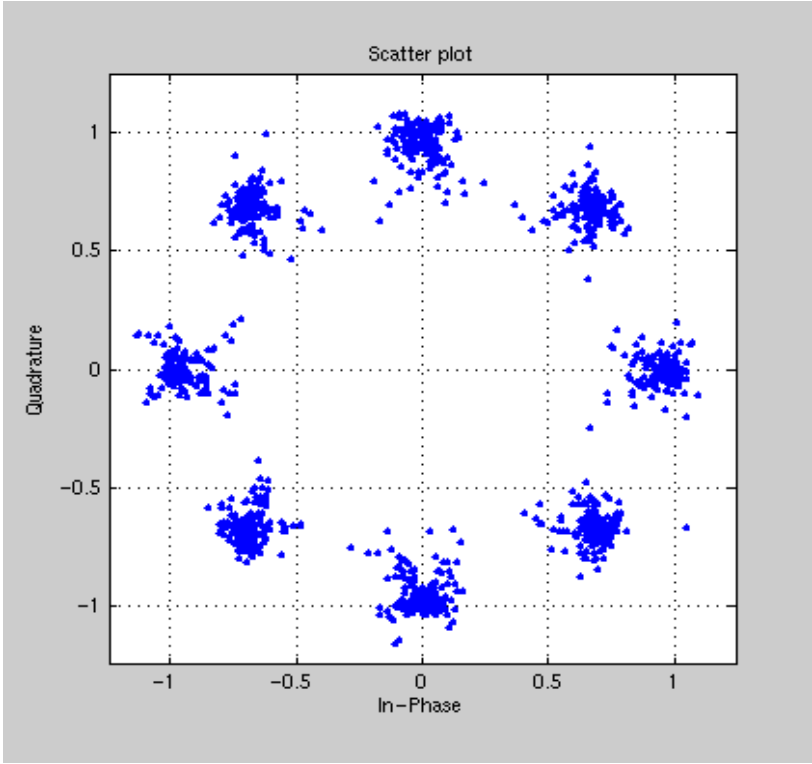
Timing Recovery - Jitter

VCO-jitter at the receiver

— colored noise with Lorentzian spectrum

Less impact of jitter

— low bit error rate at high noise



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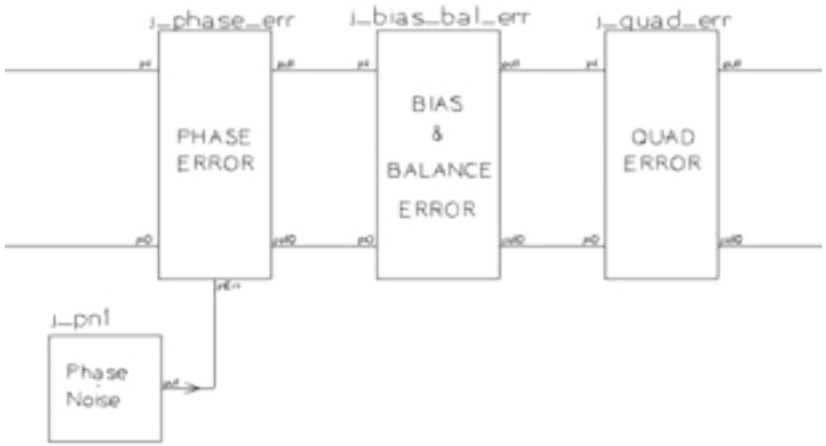
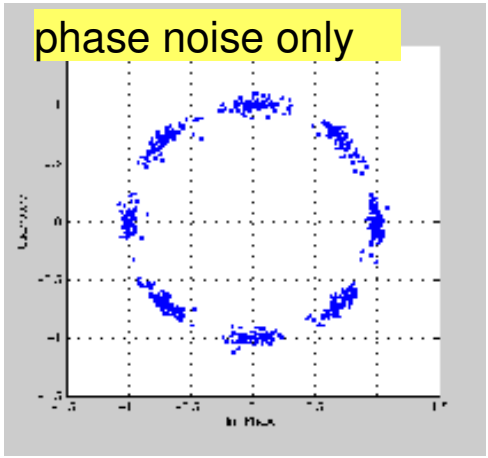
Modeling Non-idealities of the RF frontend

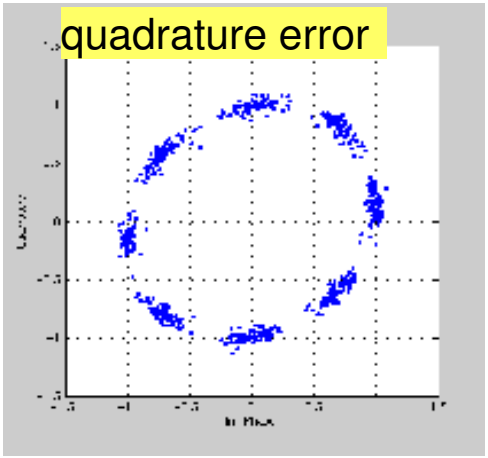
Algorithmic model
(static nonlinearities)

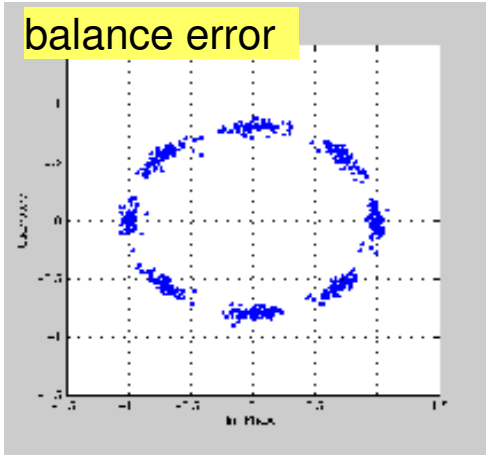
Errors can be configured by parameters to evaluate the robustness of the system against the errors

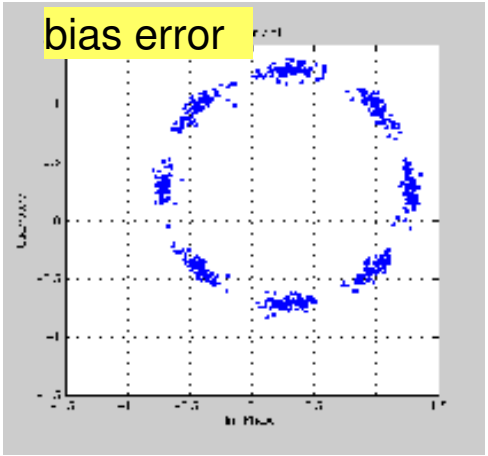


Constellation diagram









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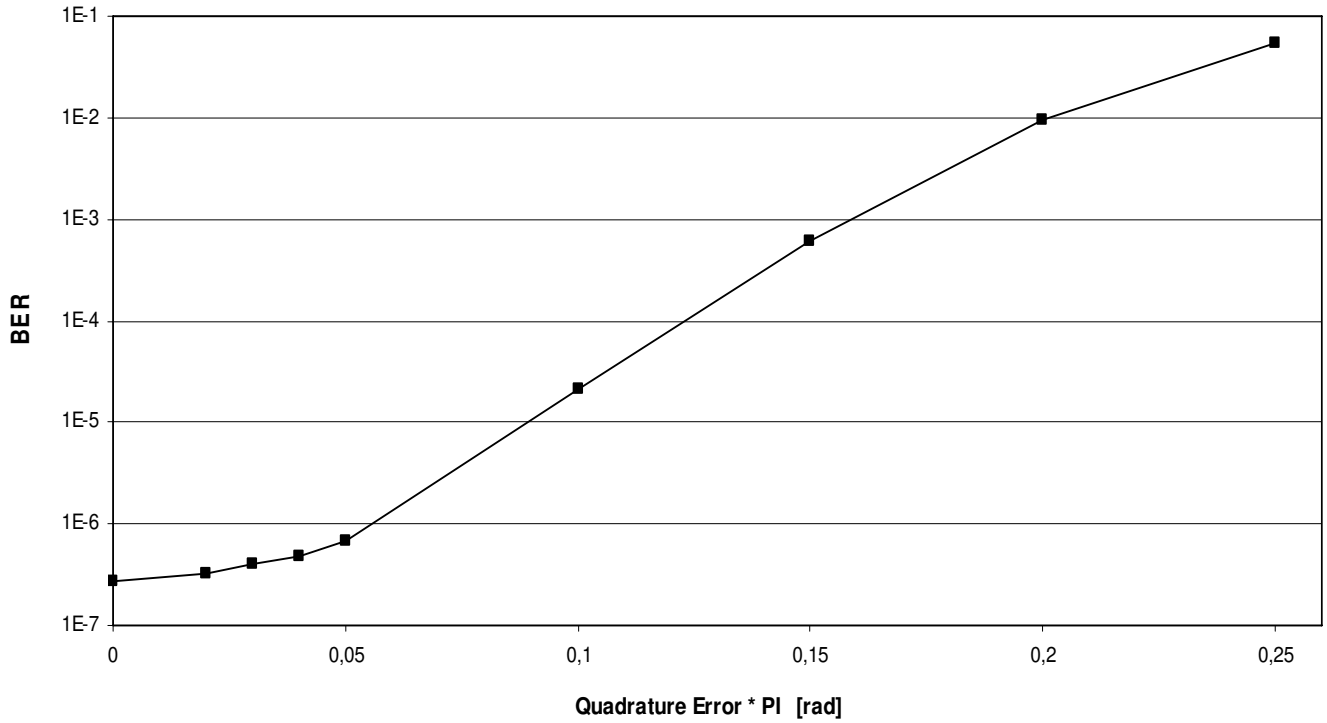
Non-idealities of the RF frontend

Analysis of bit error rates

— with phase noise

— dependent on quadrature error



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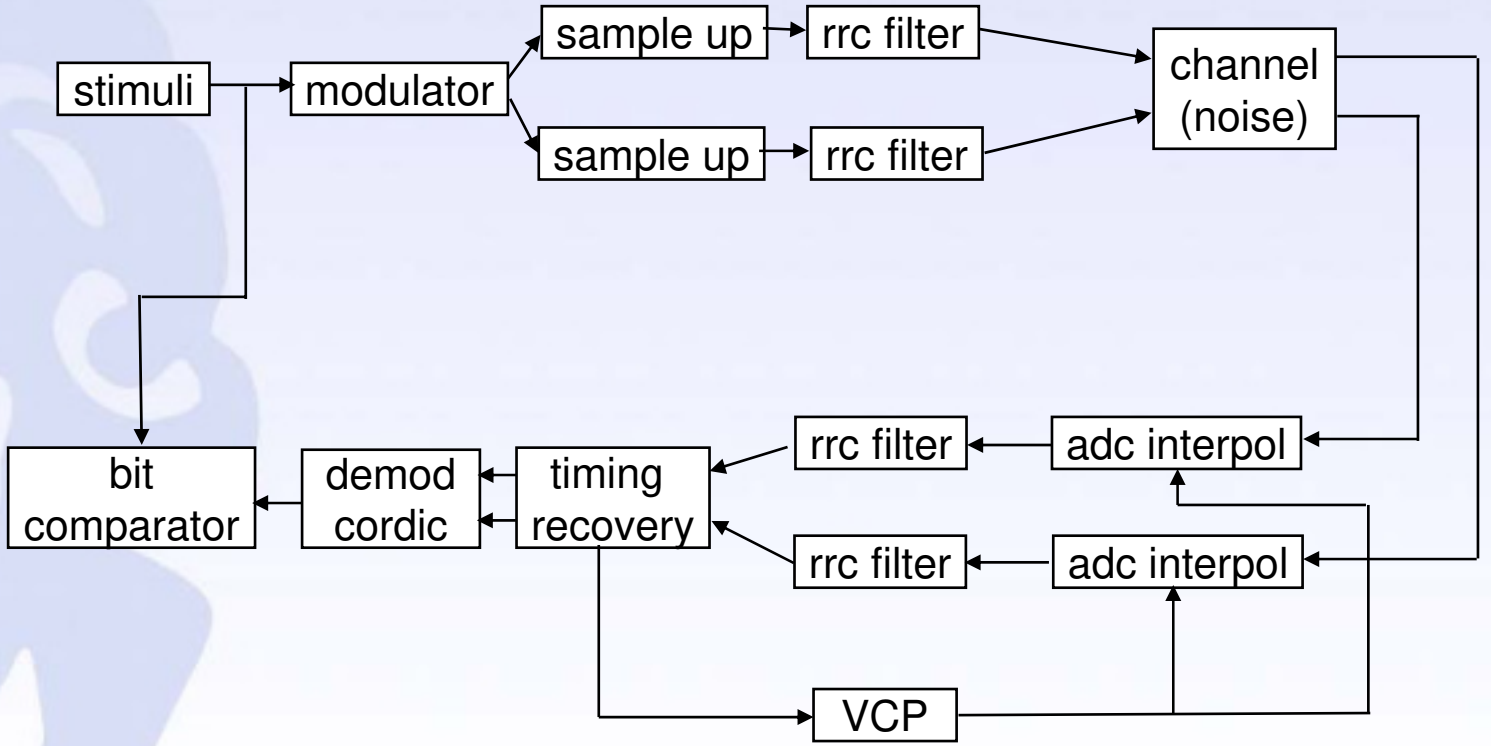
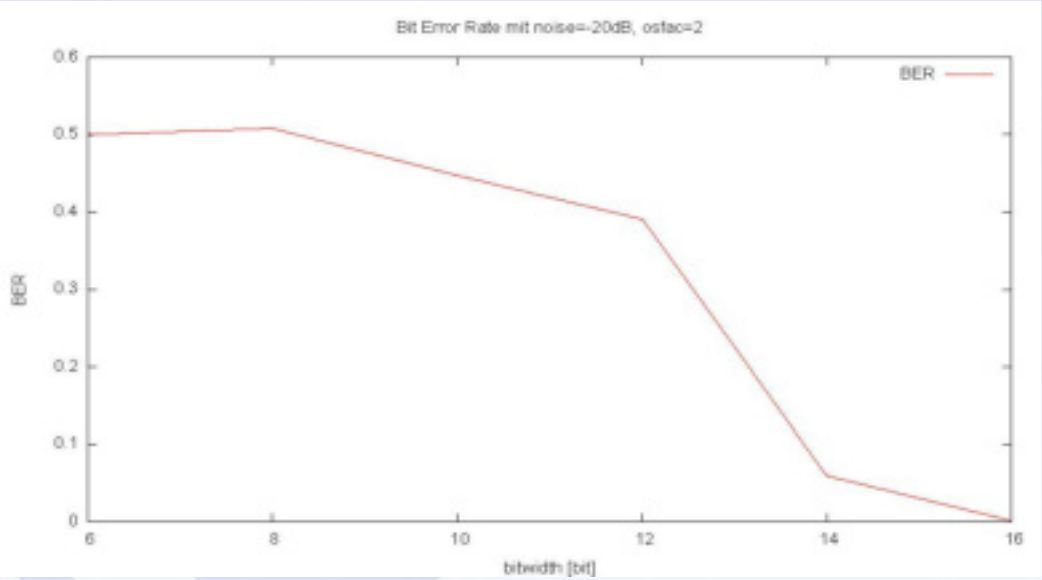
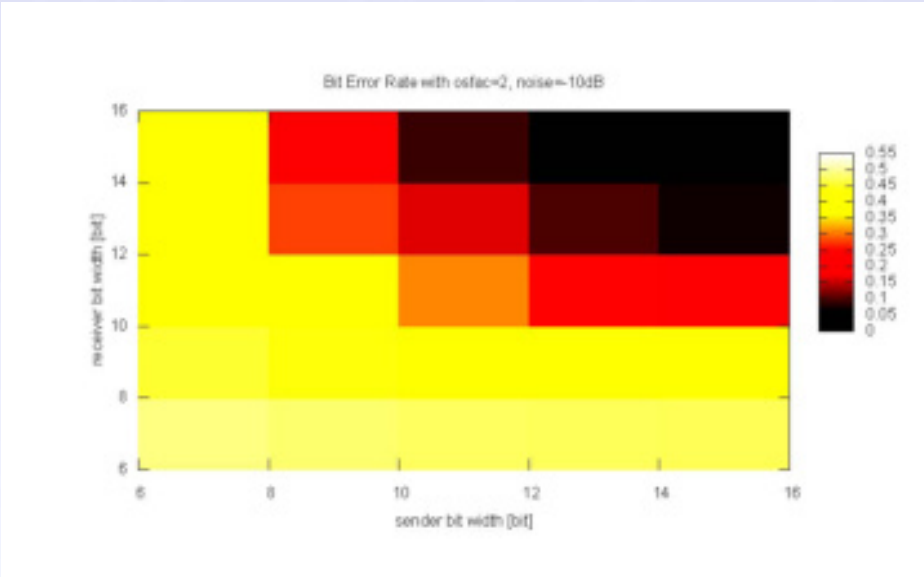
Gigabit Radio – Architectural Comparison with Polymorpic Signals



Simulation Results – Signal Width



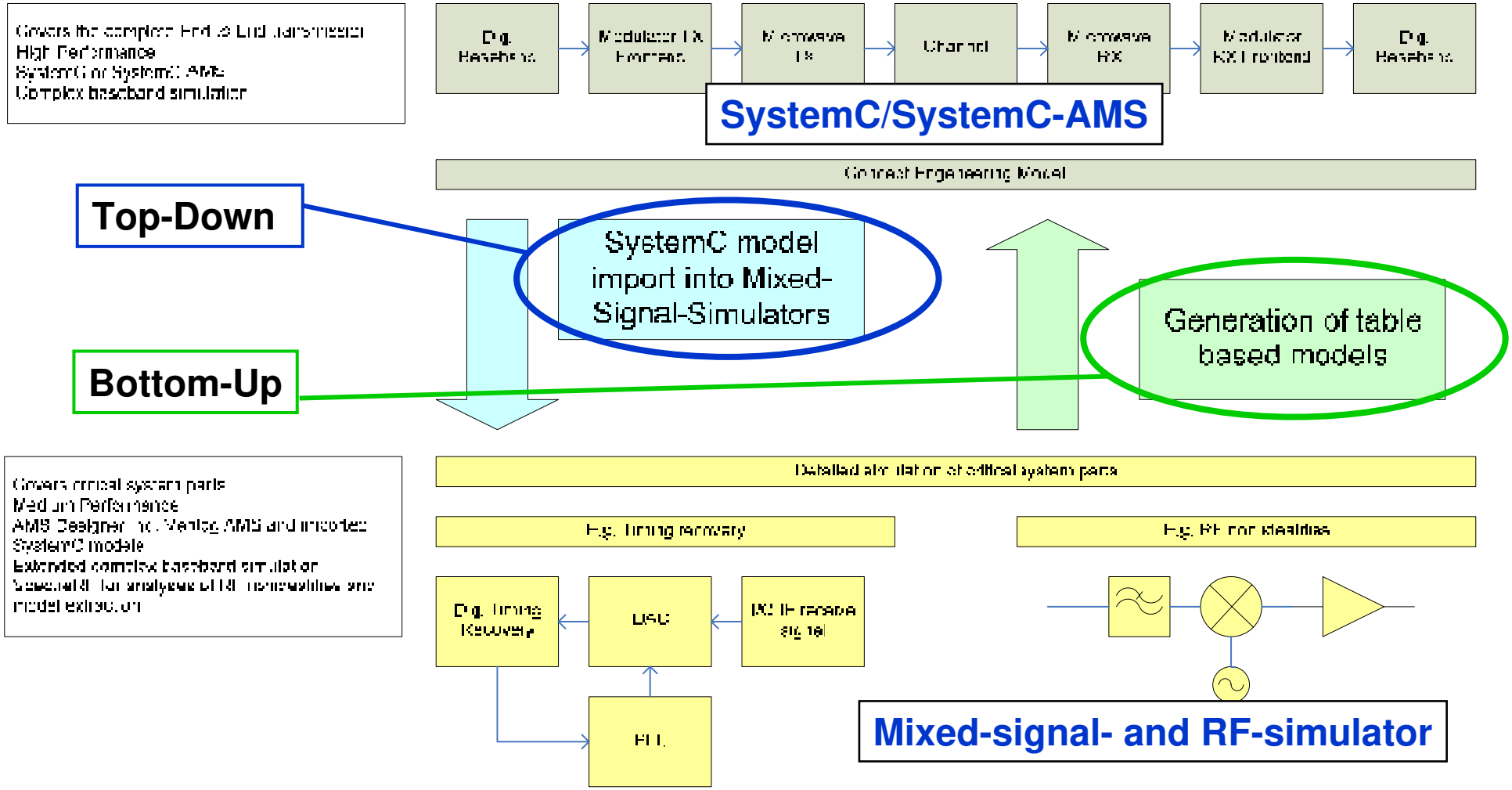


- Signal width from 6 to 16 bit

- Transmitter and receiver signal width between 6 and 16 bit

→ lower signal with required at transmitter as at receiver

Interfaces between System and Implementation



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Conclusions on System-Level-Analysis

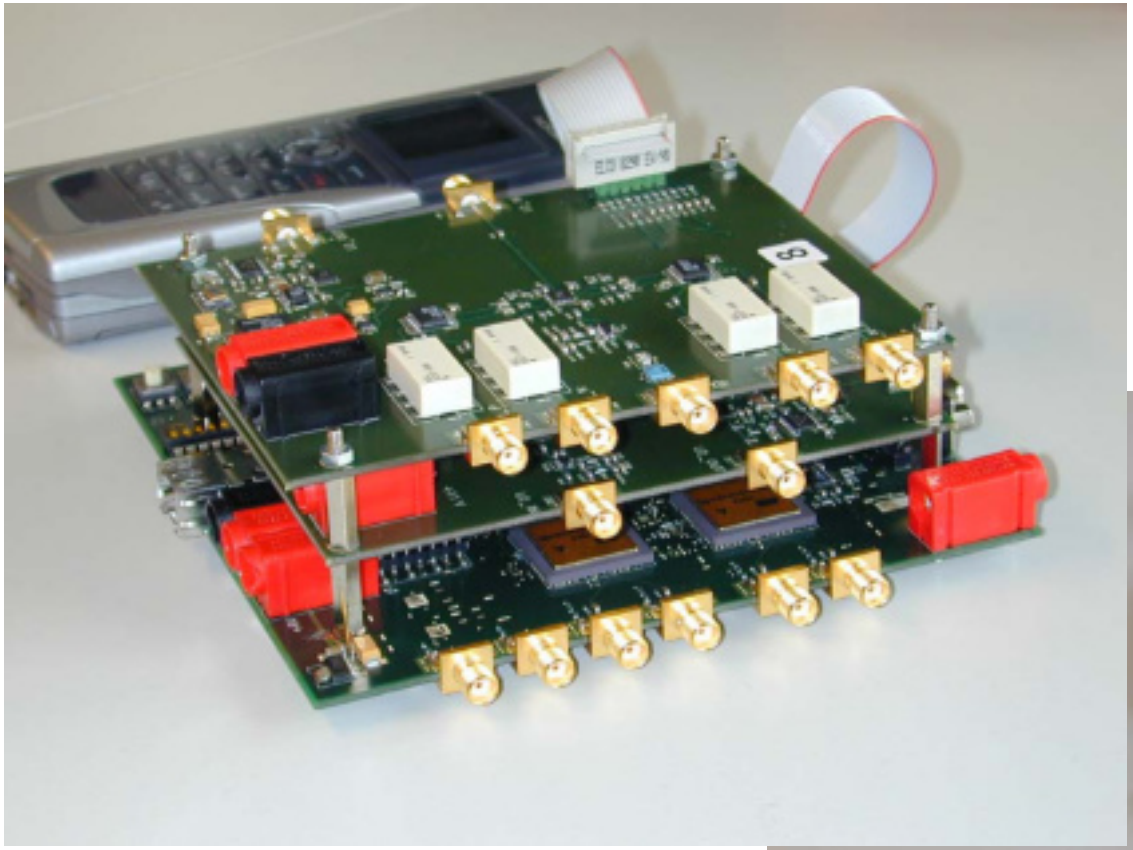
Gigabit radio was a challenge for simulation

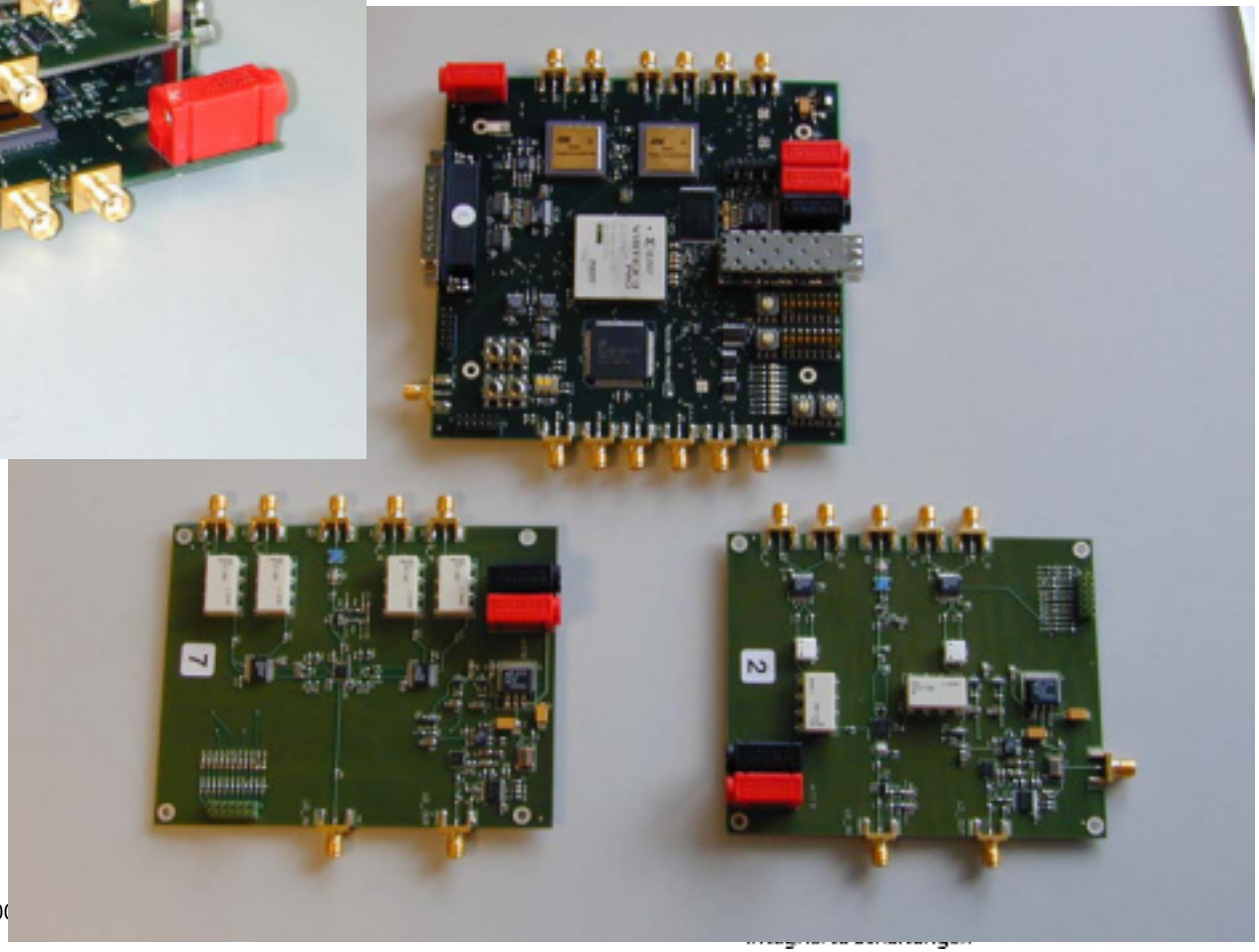
- trade-off between accuracy and simulation speed
- static dataflow provides the required performance if combined with other technologies like baseband modeling
- difficult to model analog behavior like jitter in dataflow with less overhead (mixed-signal-simulators provide better modeling capabilities in this area, but they are to slow)

What we missed

- wireless-like data visualization (eye and scatter)
- RF analyses (harmonic balance *HB* or periodic steady state *PSS*) for debugging models of RF parts

Gigabit radio modulator Hardware demonstrator and measurements

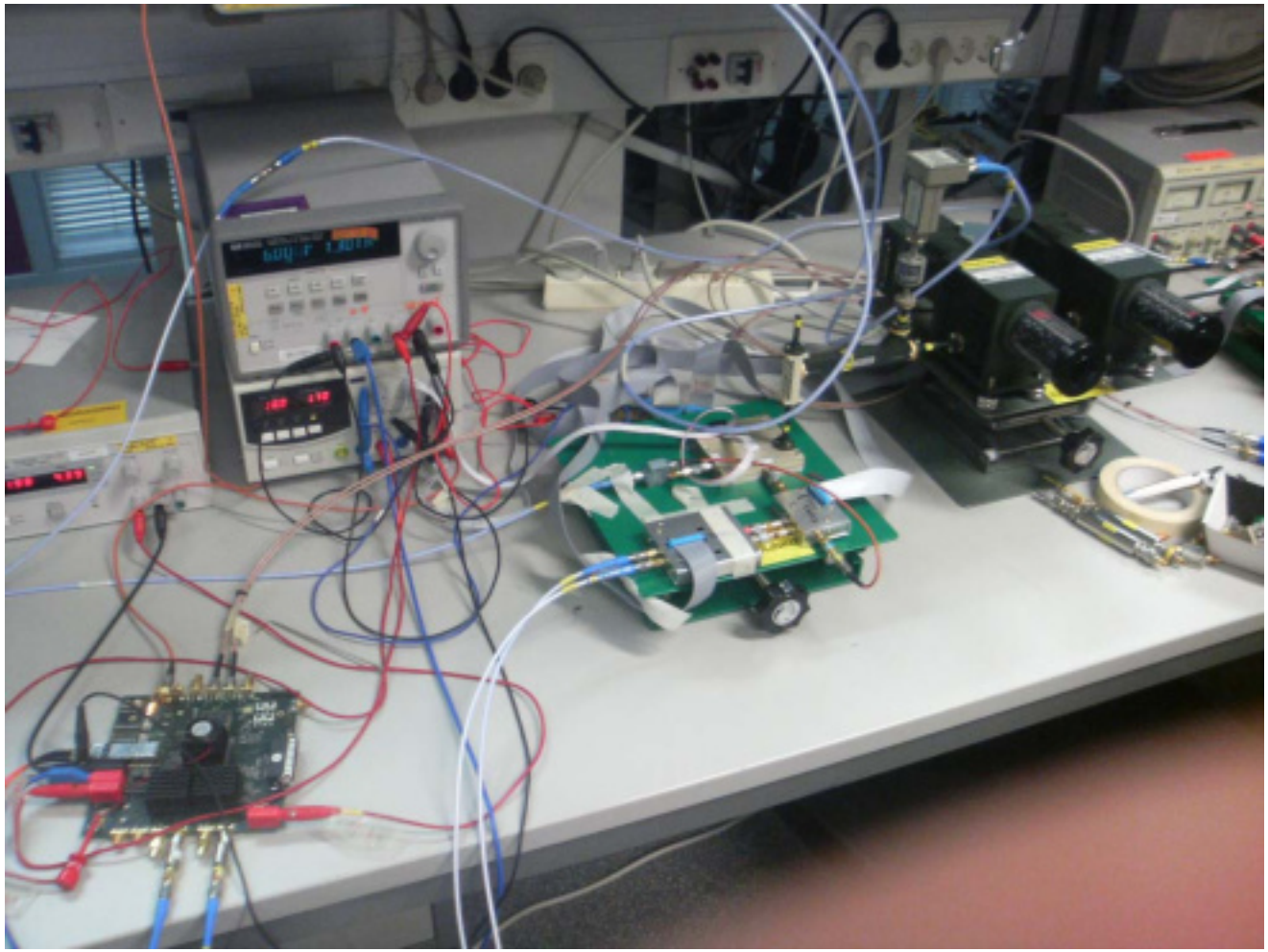




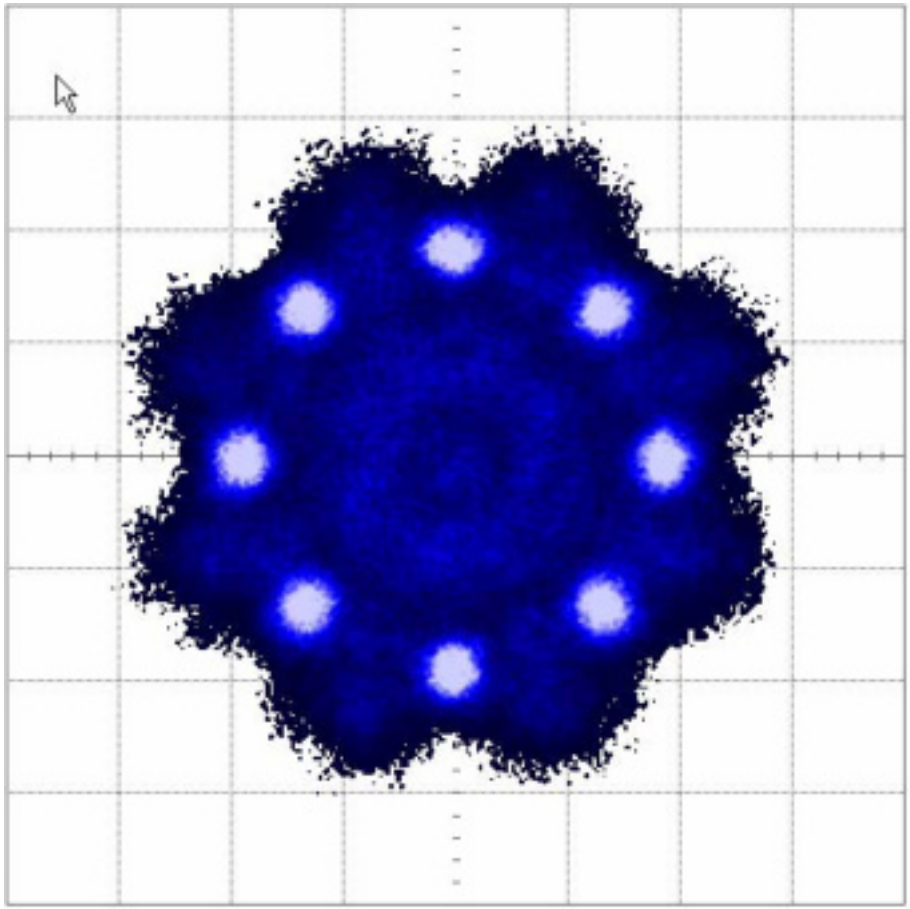
Gigabit radio link measurements

Characterization of whole Gigabit link

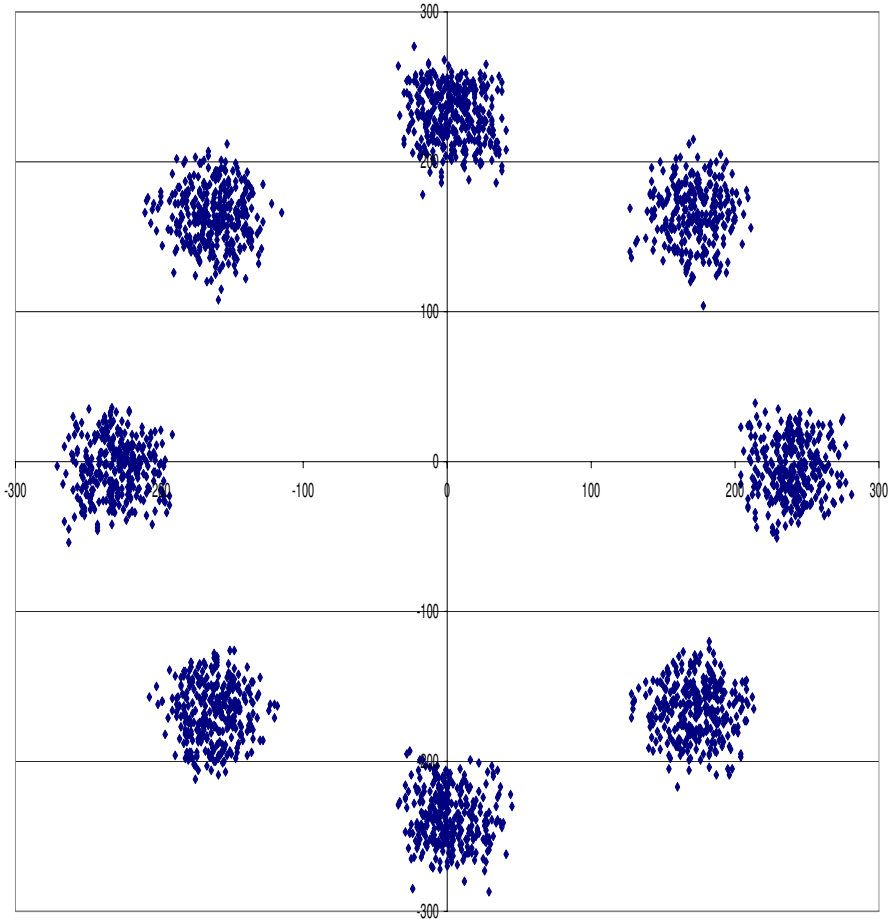
- Performed at Nokia Business Unit
- Complete radio (BB/IF/microwave/channel)
- Full functionality
- 81…84 GHz channel
- raw BER = 10e-7 … 10e-4
- modulator only with cable connection at BB:
  raw BER = 10e-11 … 10e-9



Gigabit radio link measurements



transmitted constellation diagram
(at IF)



received constellation diagram
(at BB)

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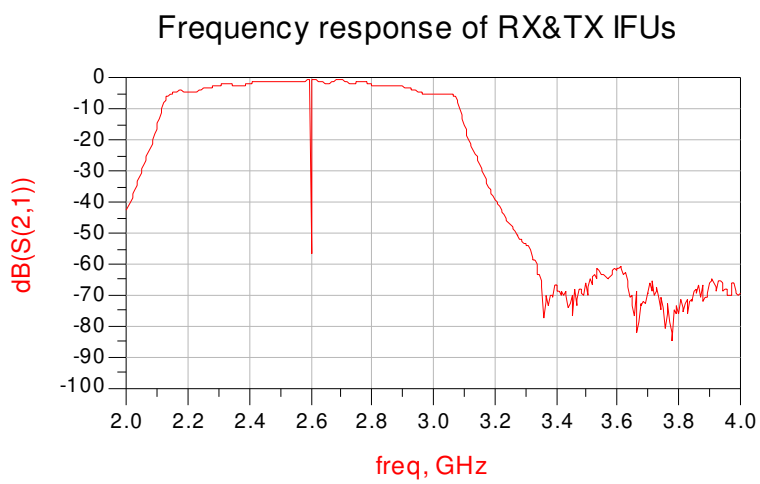
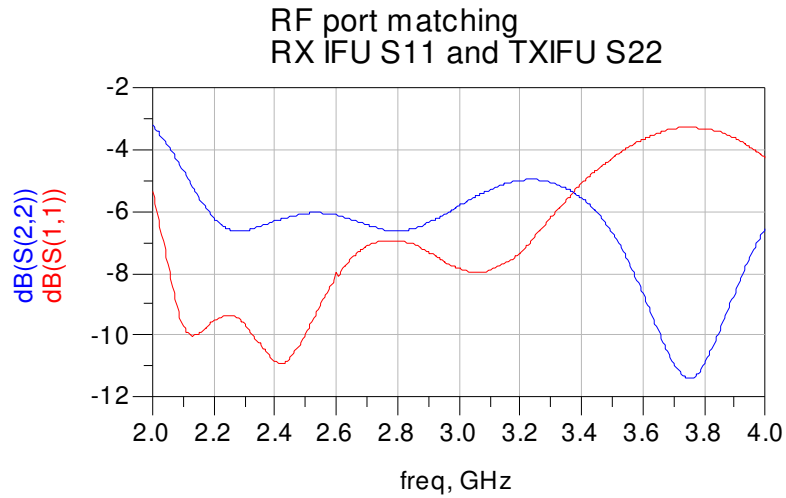
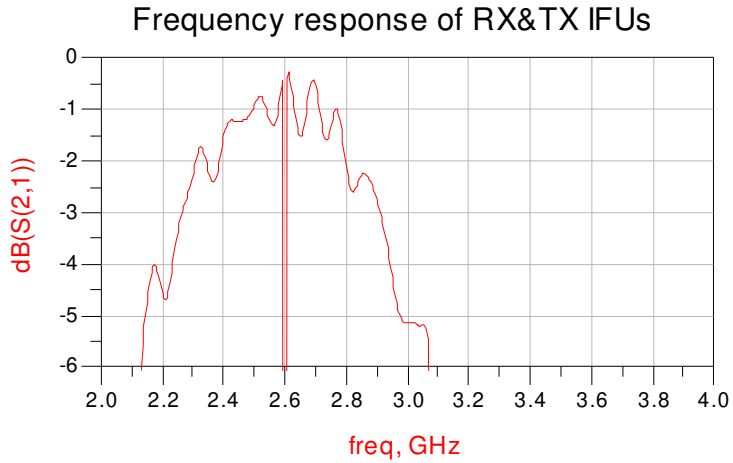
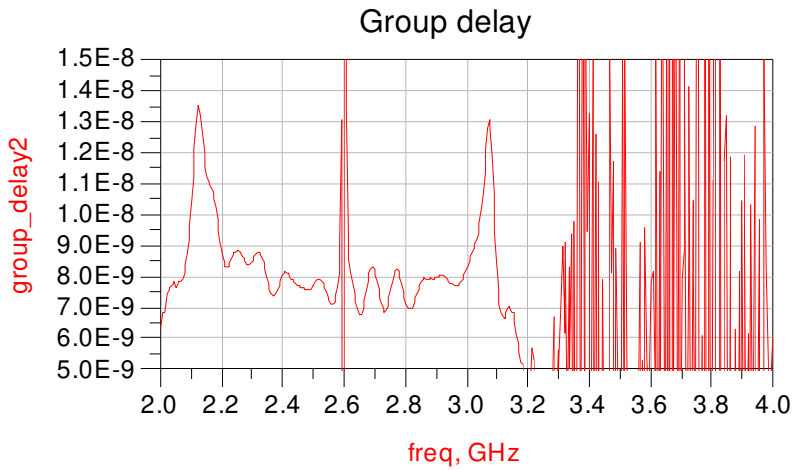
IF front-end measurement results









Fraunhofer Institut Integrierte Schaltungen

NOKIA Connecting People

Summary

- Environment for research on disruptive systems requires excellent models
  - Hard life to get a working proof of concept
  - Tight time schedules
  - Very limited budget
  - Extremely limited ressources
  - But only very poor models available for the relevant case of operation
- A variety of questions can be solved when accurate models are available
  - Dependence on transmission protocol
  - Dependence on different types of forward error correction
  - Coherent receiving
  - Does that system work at all?
- Close cooperations required to handle the challenges
  - Nokia provided selected Gigabit Radio sub-systems to research community to solve most pressing issues
  - Cooperation DETAILS – SAMS
  - Cooperation Nokia – FhG-IIS/EAS – Cadence – Univ. Frankfurt, Technische Informatik