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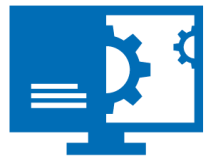


IT and Engineering

SystemC-AMS ELN: the new way of generating macro models ?

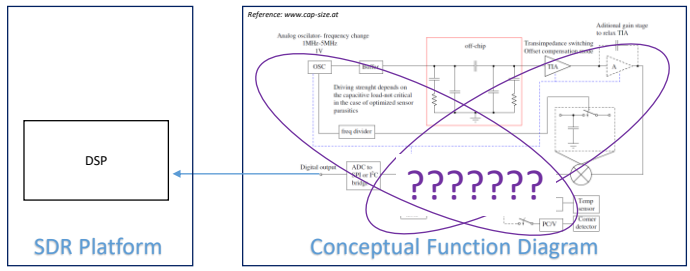
COSEDA User Group Conference
4th of November 2020, Wolfgang Scherr
Carinthia University of Applied Sciences
Integrated Systems and Circuit Design

KÄRNTEN University of Applied Sciences

Agenda

- Motivation and Background
- Alternate proposal for (board level) M/S design
- Feasibility based on some examples
- Learnings and conclusion

The need for rapid board-level prototyping



PCB prototype: performance questionable (parasitic element issues, …)

Matlab/Simulink: for initial analysis, but probably too abstract for board level model
SPICE model: feasible for analog concepts, but no exploration of alternate (digital) concepts
- can not easily include DSP part as well

Ref: https://www.cap-size.at/

Why is SPICE often the (only) choice (maybe after Matlab/Simulink) ?

- **Long history**
  - Industry: companies built up expertise and a libraries of models (= valuable IP)
  - Academics: common tool used in many curricula in electric/electronic engineering
  - Low barrier due to existing („free“) GUI simulation environments: just install & use
- Even with all this variants out there causing many compatibility problems, it is still **accepted as (quasi-)„standard“**
  → It „works“ – at least somehow and maybe after some tweaking…
- Cost vs. Benefit may not be visible enough to cause any motion towards new methodologies …
  … or to formulate it a bit provocative: ☺
  - It may be hard to convince an overstressed engineer to try something he must build up IP first.
  - Thus, it is hard to explain managers to invest money to re-do all the existing IP, training for new tools and languages, etc.

Is there a technical reason to stay on SPICE?

- Not really:
  - When SPICE is used for **virtual ESL prototyping and verification**
    - Turn-around time for architecture exploration is important
      → motivation for more efficient/faster models is anyhow higher
    - Complexity increases, including microcontrollers, DSP or FPGA components
      → mixed-mode, mixed-disciplines, multi-physics, …
    - Setups with many use cases to verify (e.g. to support requirement engineering with trace-able simulation results or regression-based testing/verification)
    - ELN simulation allows more efficient M/S modelling than RNM/EEnet discrete models (using VHDL, SV, …) with similar (and partly way faster) performance*
  - When SPICE is used to **visualize product behaviour (demonstrators)**
    - Sometimes implemented with fixed circuitry (e.g. web demonstrators), user can only vary parameters
    - Functional correctness is sufficient

** see my presentation at FDL 2020*

Is there a technical reason to stay on SPICE?

- Probably yes:
  - When SPICE is used for analysing detailed circuit behaviour
    - Detailed device models as available in SPICE required (e.g. BSIM)
    - Users can live with the simulation times, not so many design loops
    - **SystemC-AMS is no replacement for analogue circuit/device-level design tools**
  - Models used to tie customers to certain tools → **use of dedicated libraries**
    - Special elements not common to all SPICE simulators or even with proprietary functionality which is hard to translate, precompiled Verilog-A models, etc.
    - Special analysis features, monte-carlo, … including certain technology packages

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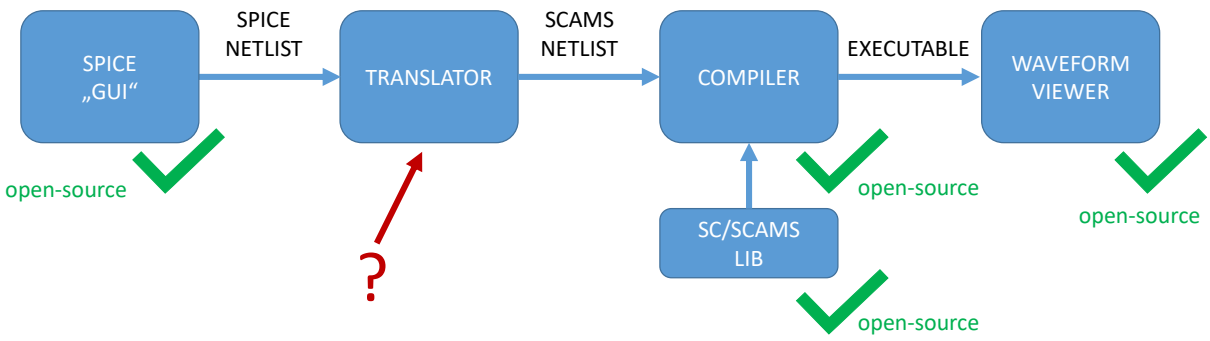
Is there something to do about it ?

- SystemC-AMS can replace SPICE in many situations on board level design
  - Provides “sufficient” similarity in terms of available library elements
  - It is a „true“ IEEE standard with an open proof-of-concept implementation
  - Several MoCs, including mixed-mode simulation, are part of the standard
- But
  - Unfortunately **no „free“ SC-AMS solution yet with graphical entry options**
    - Still quite some entry barrier to use it, especially compared to several SPICE tools
    - Thus, hand coding of netlists is still common (similar to writing SPICE netlists in the 1980s)
    - C++ coding is even more cumbersome than writing a SPICE netlist by hand

→ Idea

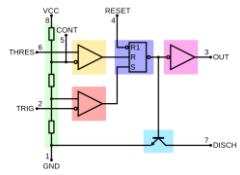
- **Take advantage of existing SPICE solutions** (= people are used to) **for SystemC-AMS**
  - Use any SPICE tool as design entry (actually only the tool to generate schematics)
  - Translate generated SPICE netlists to SystemC-AMS netlists
  - Can be also used to migrate from SPICE to SystemC-AMS and preserve generated IP
  - Must be an easy to understand process and no „rocket science“ to do the conversion

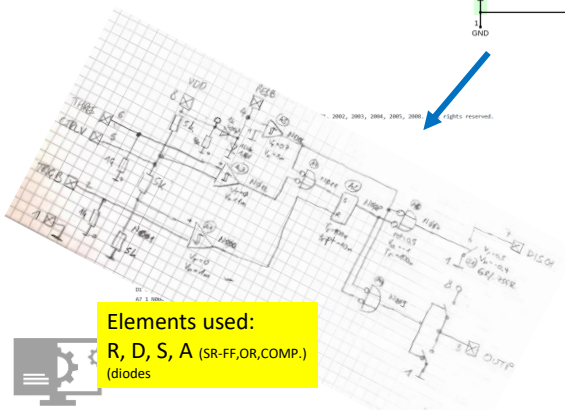
Idea

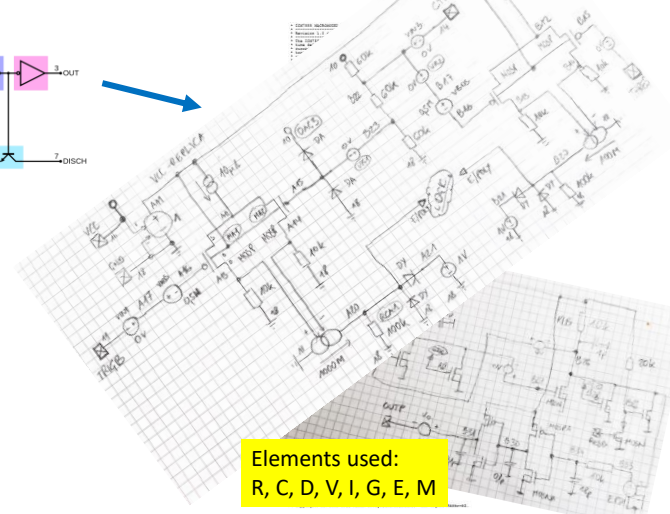


Macro model examples from the web

The „famous“ 555 timer…







Elements used:
R, D, S, A (SR-FF,OR,COMP.)
(diodes

Elements used:
R, C, D, V, I, G, E, M

Ref:
https://de.wikipedia.org/wiki/NE555#/media/Datei:NE555_Bloc_Diagram.svg
https://www.maximintegrated.com/content/dam/files/design/tools/modeling-simulation/spice/timers-counters/macro/icm7555.fam
https://github.com/knightshrub/Spice-models/blob/master/sub/NE555.sub

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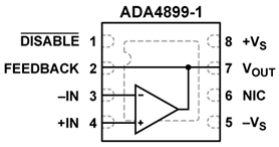
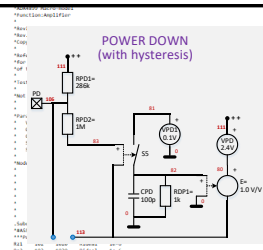
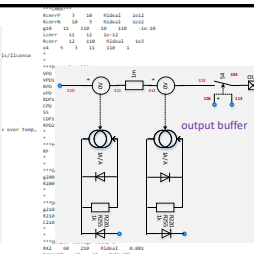
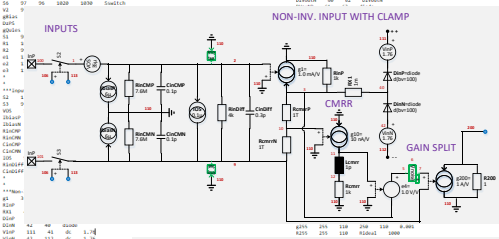
Opamp model

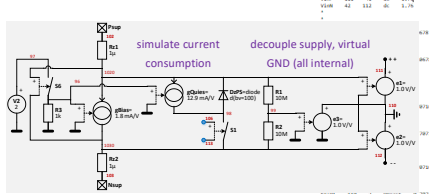


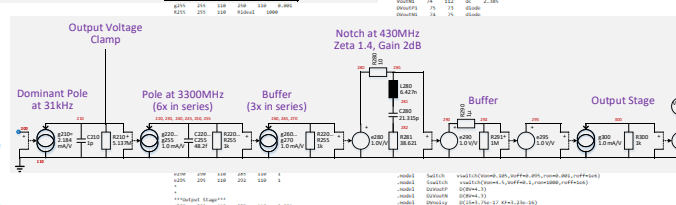






Elements used:
R, C, L, D, V, I, G, E





Ref: https://www.analog.com/en/products/ada4899-1.html

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Proposed translation procedure

- Passive elements and independent sources can be translated automatically
- Dependent sources, diodes, transistors to be replaced by PWL sources
  - Needs to generate a library with some basic elements
  - Except very special sources (e.g. polynomial, rarely used in models anyway)
- Special elements (Axxxx) can be replaced by embedded TDF functions
  - Again, needs to generate a library with some basic elements
- Notify used for not translated lines, show SPICE line with translated signal names (for easier manual adaption of the SystemC-AMS code)

General observations

- Models are often „flat“ netlist structures with 10…250 lines
  - Simple to translate
- SPICE naming conventions on signal and instance names need translation
  - Need proper translation (also to simplify debugging / traceback to netlist)
- Internal „zero-time“ signal feedbacks may cause issues, requires manual work
- Some models use switches → anyhow not optimal for a SPICE simulator…
- Nonlinear models (M, D, …) are often used with default model cards, but maybe one or two parameter changed
  - It can be assumed that the model is not really accurately set up, translation to a linear model should not show a significant overall deviation (at least a good starting point can be generated)
- Sometimes models are not at all properly done and way too complicated
  - or “amateurish” - even if they are found on respected AMS semiconductor pages…

Problem of „SPICE“ (in)compatibility…

„Basic standard“ models … … … „Dedicated“ models

(and probably widely use-able) (and probably limited to specific tools)

.) close to „original“ Berkeley SPICE
.) mainly passive, linear elements
.) linear controlled sources
.) non-linearities using diodes as simple „switches“ etc.
.) sometimes also suited for AC analysis (small-signal)

→ Likely to work with an auto-translation

.) special or proprietary models (e.g. Axxxx elements, Verilog-A)
.) PWL and similar controlled sources
.) transistor models with special model cards
.) usually only large-signal / transient simulations

→ Will need manual corrections

Example: Diode model (forward only)

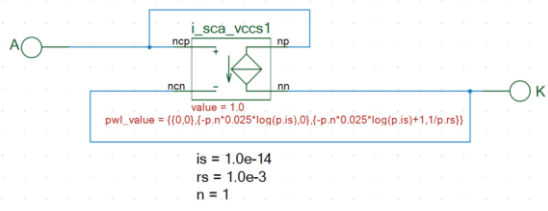
- Found in macro model:

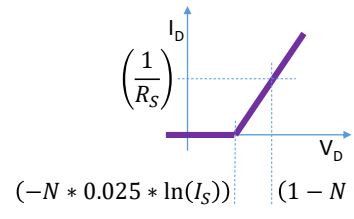
```
.MODEL DA D(IS=100E-14 RS=0.5k)
.MODEL DX D(IS=100E-14)
.MODEL DZ D(N=10M)
.MODEL DY D(IS=100E-14 N=0.1M)
```

Berkeley SPICE diode
(simplified, based on Shockley eq.)

$$I_D = I_S\left(e^{\frac{V_D}{N \cdot V_t}} - 1\right)$$

- SystemC-AMS ELN model proposal (using an PWL-VCCS*)



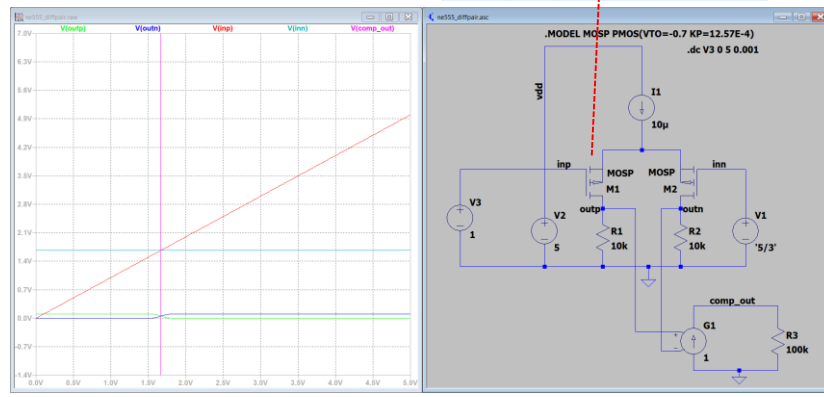


** already part of POC-implementation, subject to next IEEEE1666.1 standardisation*

Would an automatic translation succeed?

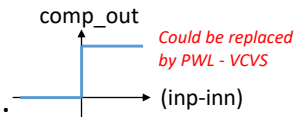
- Example macro model translation – differential pair:

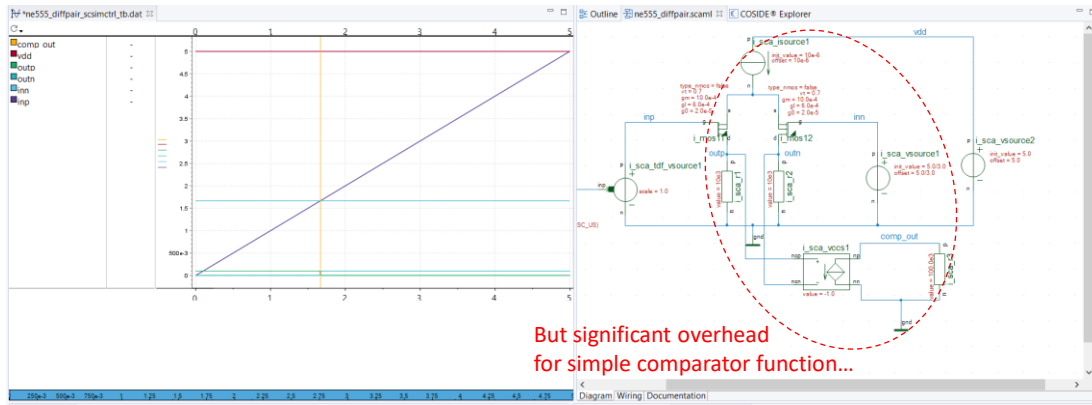
- Unnecessarily complex macro model, so good "worst case" example
- Model of M1/M2 not really important
- Use automatic translation using a simple "default" model (using Coseda mos1 model with gl = gm = kp and vt = vto)



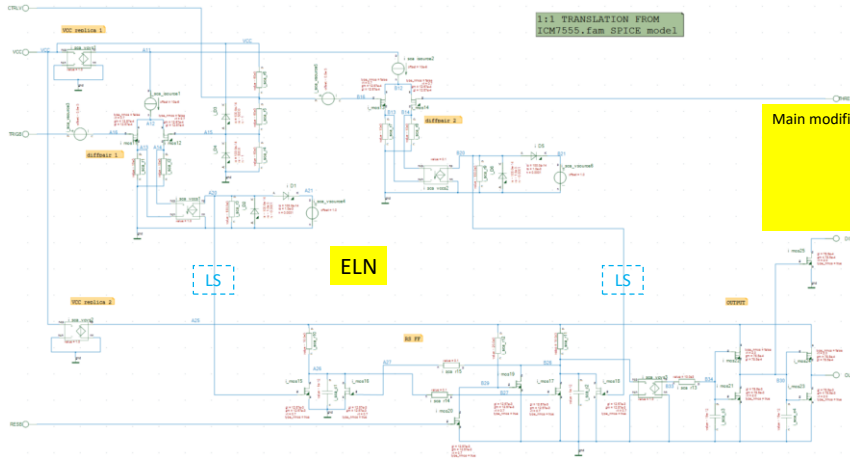
How the translation could look like

- The „default translation" fits quite well for the example…

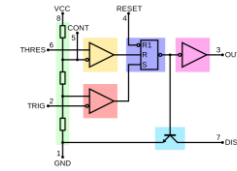




A „inefficient SPICE example“ of a 555 timer macro model, translated to SystemC-AMS



Main modifications:
.) 0V-DC sources removed
.) 2.O. polynomial VCVS (level shifter) removed
(note: VCVS is general not a good idea to use in SPICE...)
.) Simplified diode and transistor models



Ref: https://de.wikipedia.org/wiki/NE555#/media/Datei:NE555_Bloc_Diagram.svg

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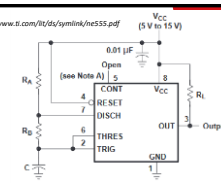
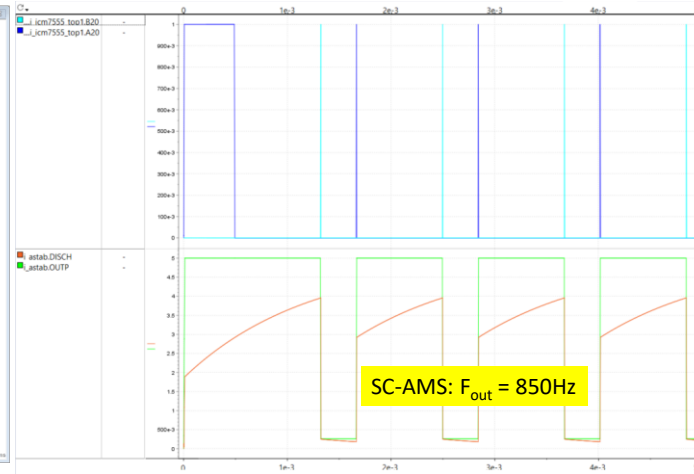
LTSpice versus SystemC-AMS

Ref: https://www.ti.com/lit/ds/symlink/ne555.pdf



Expected from datasheet formulas: F_{out} = 872Hz

SPICE: F_{out} = 867Hz



SC-AMS: F_{out} = 850Hz

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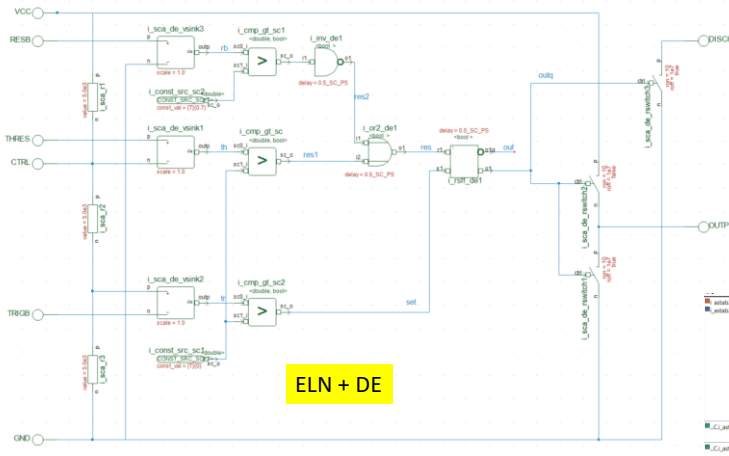
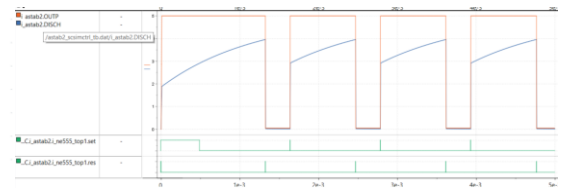
Simple NE555 SPICE model translation → much less complex, similar results



Expected from datasheet formulas: F_{out} = 872Hz

SC-AMS: F_{out} = 871Hz



Main modifications:
.) own DE models for Axxxx elements
.) schematic modified for presentation purposes

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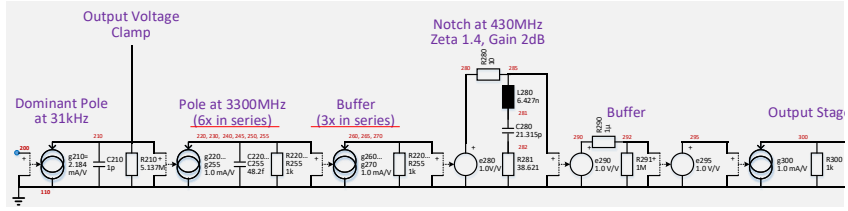
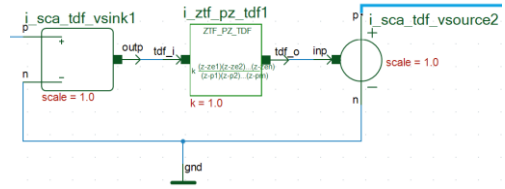
Example for SC-AMS optimisations

- Operational amplifier frequency behaviour macro model



- Could be replaced by one ZP/ND element via TDF



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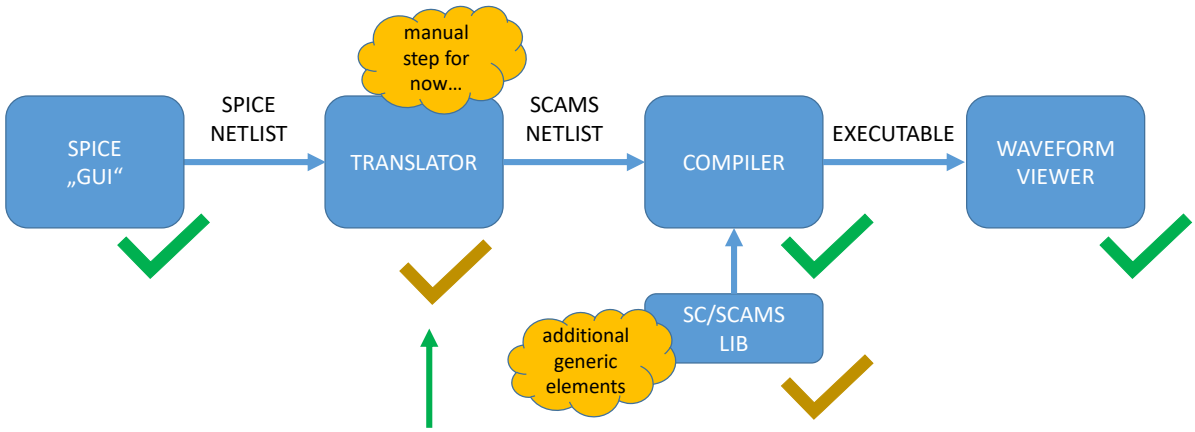
Feasibility (exemplary)



R,L,C,V,I,E,G,A,D,M

May need SC-AMS extension as part of the PoC library, but not (yet) part of the IEEE standard

How to verify

- Testbenches and test cases can be written in SPICE (and probably already exist in SPICE)
- Can be translated as well to SystemC-AMS as starting point
- With SystemC(-AMS), more sophisticated verification techniques may be used later on
- COSIDE would also offer NGspice integration (proprietary method)

Conclusion & Outlook

- Automatic translation should be possible in principle for many models with low effort to generate
  → **straight-forward and easy to use tool/process** for designers
- A translator fulfils the purpose/idea of an initial, entry-level, low cost design flow
  → **SPICE is only used as "schematic entry / GUI" for SystemC-AMS**
  → when the value is recognized, next step is the value of automatic code generation and further functions offered by tools like COSIDE
- It helps to get used to the possibilities of SystemC-AMS
  → new models can **use other MoCs available in SystemC-AMS**
- Several models under investigation could be implemented way more efficiently even in SPICE – what is "a bad model" will be also a "bad model" after a 1:1 translation
  → but it was used before that way, so there might be other reasons
- Recognising certain circuit structures (e.g. generate graph of netlist and try to match subgraphs) may help in the translation process by providing hints for model improvements or replace parts automatically (user decision!)
  → **can help designers to improve models** in general
  → can help to point out further SystemC/SystemC-AMS features

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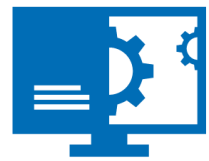

THANK YOU FOR YOUR ATTENTION

And thanks to COSEDA Technologies GmbH for their tooling and support!