# SystemC AMS Day 2011

*Industry Adoption of the SystemC AMS Standard*

BLOCK 2: SYSTEMC AMS FOR AUTOMOTIVE AND SENSORS SEMICONDUCTOR INDUSTRY

**An Efficient Transceiver Design Verification Method by Means of SystemC AMS – VHDL Co-simulation**

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This abstract deals with efficient digital design verification focusing transceiver ASIC development. This is achieved by co-simulation of SystemC AMS and VHDL. The basic motivation for using SystemC AMS is to reduce design and verification cycles by speeding-up simulation runs. In this context we introduce SystemC AMS modeling on a high abstraction level. The main target here is control path verification by analog front-end data path abstraction. Hence, we introduce so-called “Virtual Data Path” (VDP) modeling comprising only signal parameters passed between modules, not the signal itself. Main signal parameters are signal frequency and signal strength. One could also consider signal offset, signal phase and additional information, too. The front-end modules are kept as simple as possible, keeping their core functionality to a reasonable degree. At the interfaces to the digital domain real signals are generated from the respective signal parameters.

Additionally, by a proper choice of the cluster sampling time, also depending on the test case, simulation speed can be (positively) influenced. For sure we have to find a trade-off between simulation performance and timing accuracy. Simulation performance is also influenced by the number of module calls. We try to reduce it by integrating as much functionality as possible into the modules. As an outlook it is planned to do transceiver performance/sensitivity simulations. As an efficient modeling technique for that equivalent lowpass representation of the analog front-end data path is planned. Further, a combination of VDP and equivalent lowpass modeling towards multi-level simulation is targeted.