SystemC-AMS Modeling at Infineon Technologies Austria - COM

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WIRELINE COMMUNICATION SYSTEM:
The requirements of a whole Voice over IP (VOIP) system setup for Customer Premises Equipment (CPE) is presented. The Infineon VINETIC 2VIP product and the required SystemC-AMS-Model is presented in detail.
The System consists of the Transmission-Line using Resistors and Capacitances including Protection circuits.
A high voltage driver (HV-SLIC) is used to control the transmission line.
The modeling of the ADC and DAC using transfer-function, Noise-Shaping and different noise models is shown.
The digital filter part is modeled in static data flow (SDF) to cope with the change of data-rate.
The way to model the used hardware-processors and the according C-Code firmware of the processors and the inclusion of them in the SystemC-AMS simulation is shown.
The parallel usage of static data flow and standard SystemC event driven signals is also used for modeling the DCDC converter in the system.

As summary a collection of all requirements and up to now used solutions including possible improvements will be given.

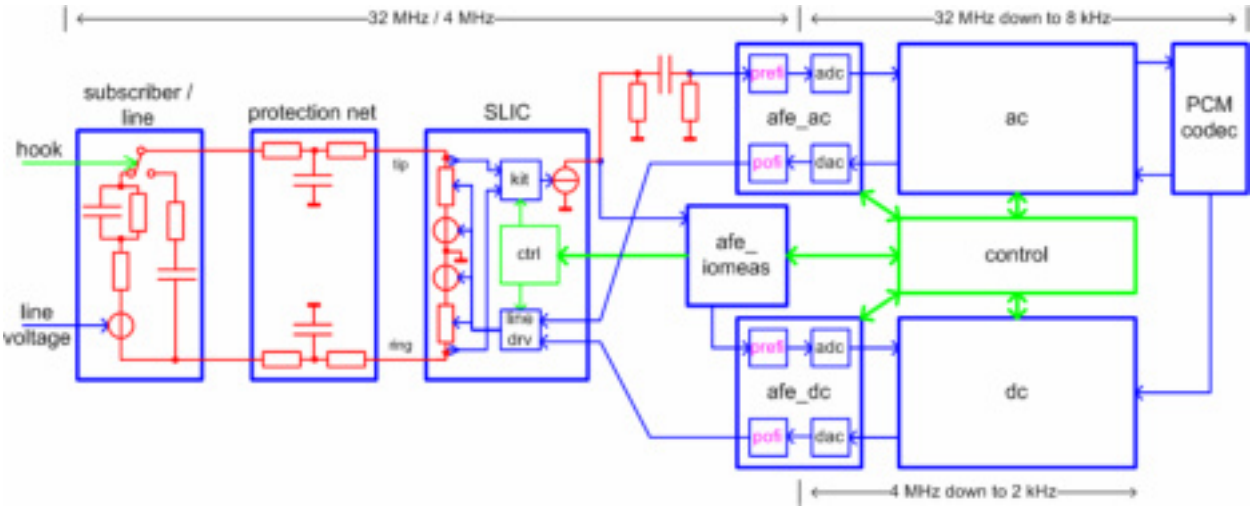


Fig. 1: VINETIC Voice over IP System.

C/C++-Based Modelling of Embedded Mixed-Signal Systems

SystemC-AMS Modelling for Voice over IP Physical Interfaces

Dresden, June 25th and 26th, 2007

Gerhard Nössing
Infineon Technologies Austria AG Villach

Never stop thinking

Gerhard Nössing

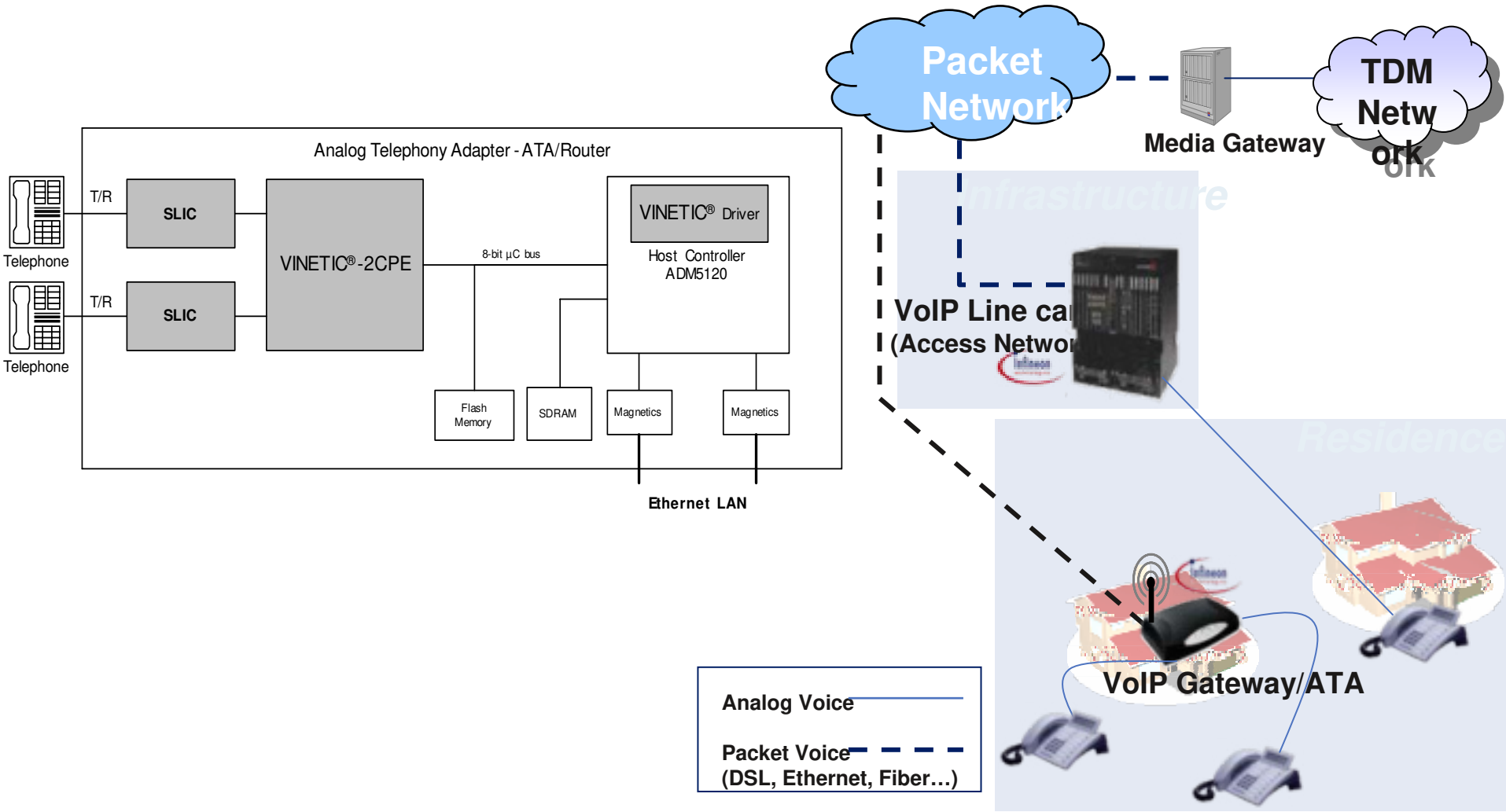
- Working since 1997 for the Design Center Villach
  - Diploma theses was dealing with V.34 Modems
  - Concept Engineer for POTS codecs
  - Concept Engineer for ADSL CO AFE
  - System Architect for POTS System

- Main Topics regarding Modeling and Simulation
  - System Modeling in Matlab, Simulink and COSSAP (before 2001)
  - Since 2000 we were working together with FHG Dresden on the development of SystemC-AMS (MEDEA Anastasia Project)
  - Member of OSCI SystemC-AMS working group

Reasons to use SystemC for Modeling of Analog / Mixed Signal Systems

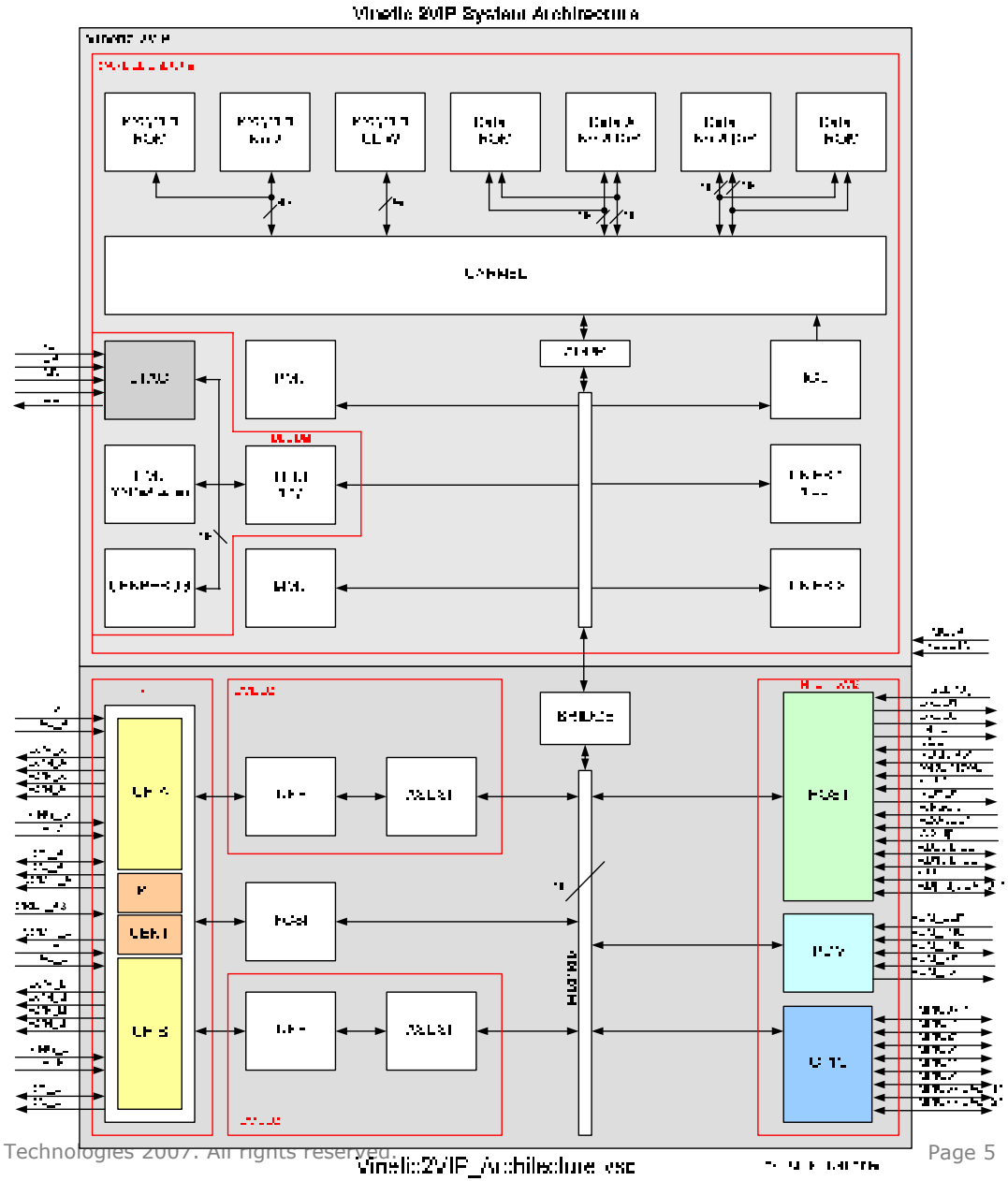
- Prototype / Executable Specification
- High Abstraction Possible
  - Fast Simulation
  - Ready to handle complex Systems
- Based on C/C++
  - Most Processor Cores have a C compiler
  - Coupling to a lot of tools
- Easy Link to Digital Design
- Mix different Models of Computation
- IP Protection and Model Exchange

Example POTS System Vinetic 2CPE

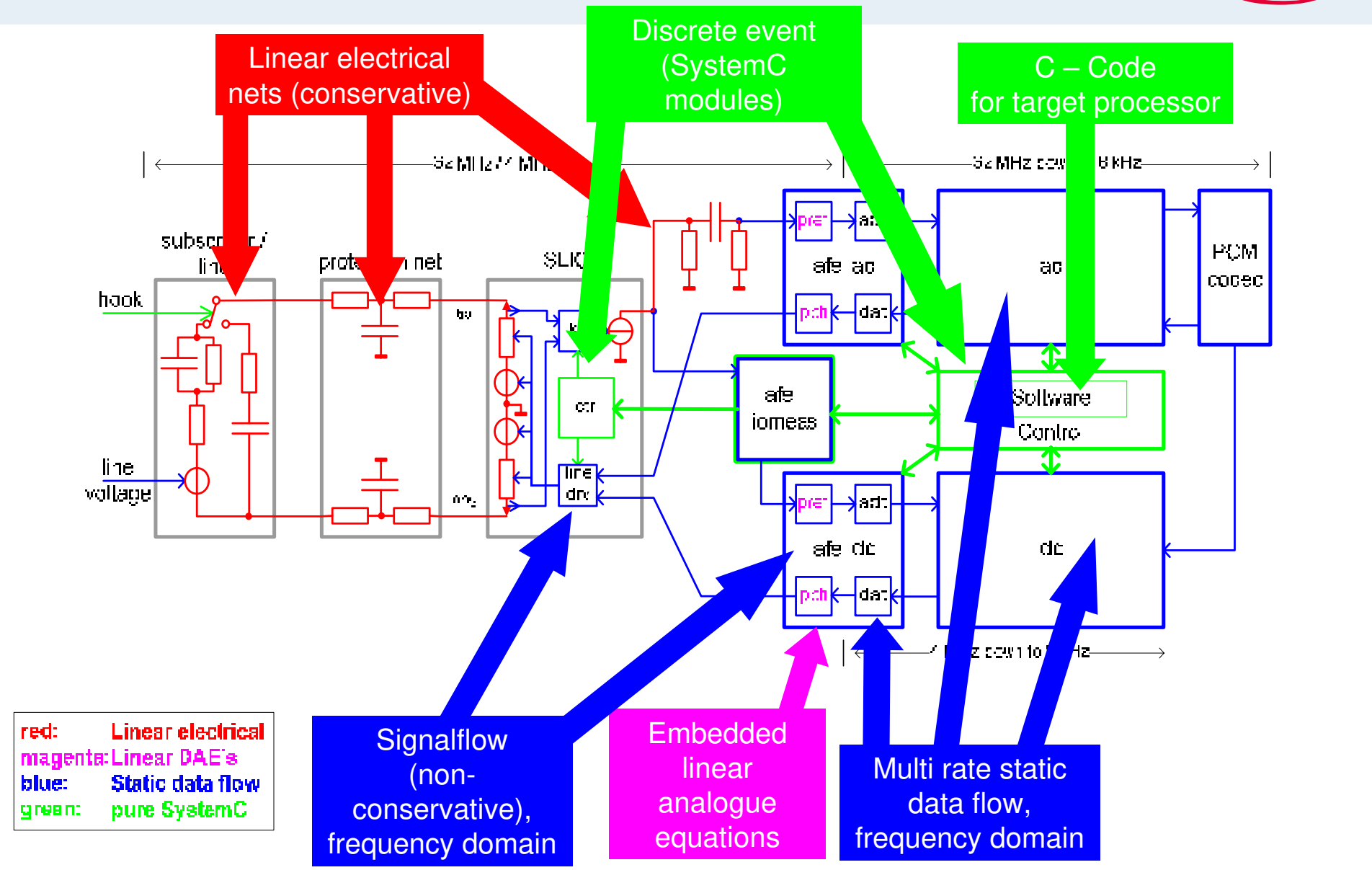


Vinetic-2CPE

- Digital Signal processing based on ASDSP and HW filters
- Carmel Subsystem (including PROM, PRAM, DROM, DRAM)
- Total Memory: 4,4Mbit (53 blocks)
- Host Interface (serial and 8bit Interface, PCM)
- Analog macro incl. PLL
- Clock frequency: 164MHz



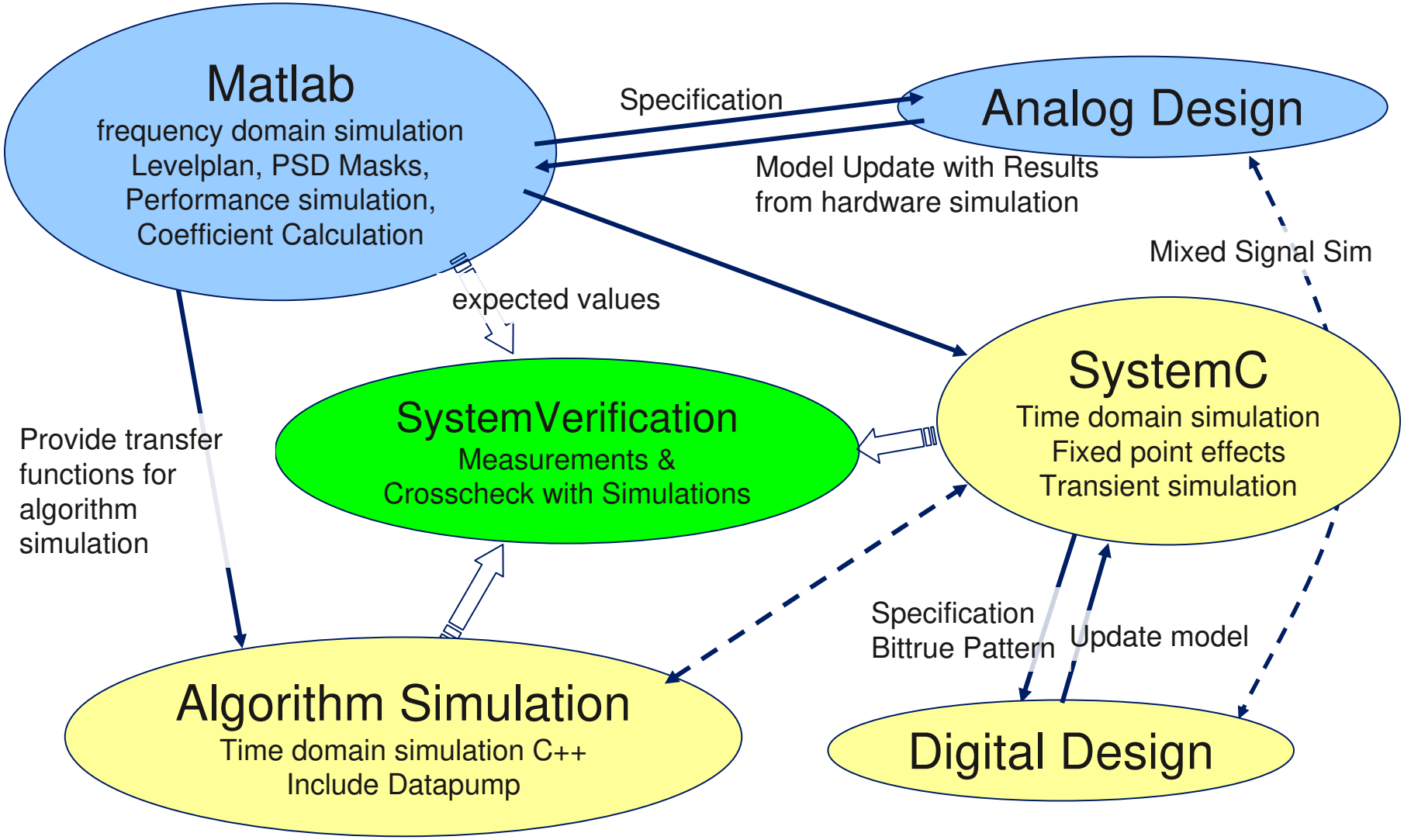
Application of different analog MoC



Simulation Time for Vinetic 2CPE System

- SystemC-AMS Simulation
  - 2 channel including: SLIC, externals, AFE, DFE, ASDSP and part of Carmel FW
  - 1 sec realtime ➔ 1,5h simulation time
- VHDL RTL
  - 2 channel including: AFE, DFE, ASDSP, Carmel and Interfaces
  - 1 sec realtime ➔ 300h simulation time
- Nano Sim (Fast CMOS simulator)
  - 2 channel including: AFE top level
  - 1 ms realtime ➔ 15h simulation time
- Titan Simulation
  - 2 channel including: AFE top level
  - 1 ms realtime ➔ 500h simulation time
- SystemC-AMS Simulation for Duslic-XT
  - only one channel
  - reduce sampling rate for analog blocks (used for FW simulation only)
  - 1sec realtime ➔ 90 sec simulation time

System Simulation and Verification approach



VINETIC 2CPE SE overall workflow

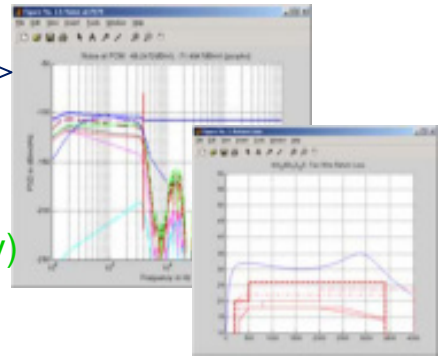
Requirements

Specification

Analog Design

del (only frequency domain)

plots of
Return Loss
RX, TX, TH
Nyquist (Stability)
Noise, OOB



legend:

red: interfaces to other BU
blue: our workflow
green: our outputs

Module Specification / DTD

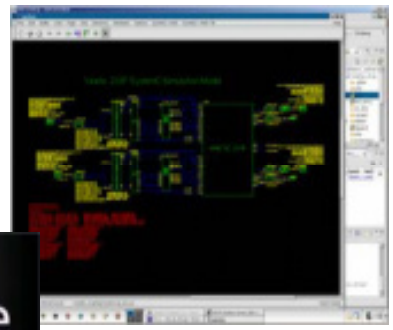
Adobe FrameMaker 7.1

*.xml

Dig Design

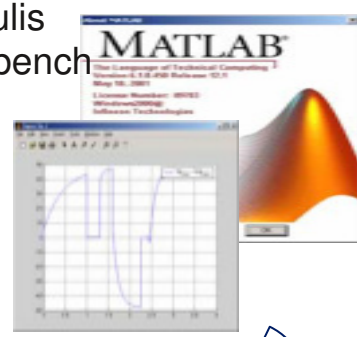
Coefficients

Cross checks of SystemC time domain via FFT with Matlab frequency domain



Defining Stimulis for global testbench

Tracefiles



XML.ORG

*.h, *.cpp
*.sym
*.fm, *.svg

eclipse

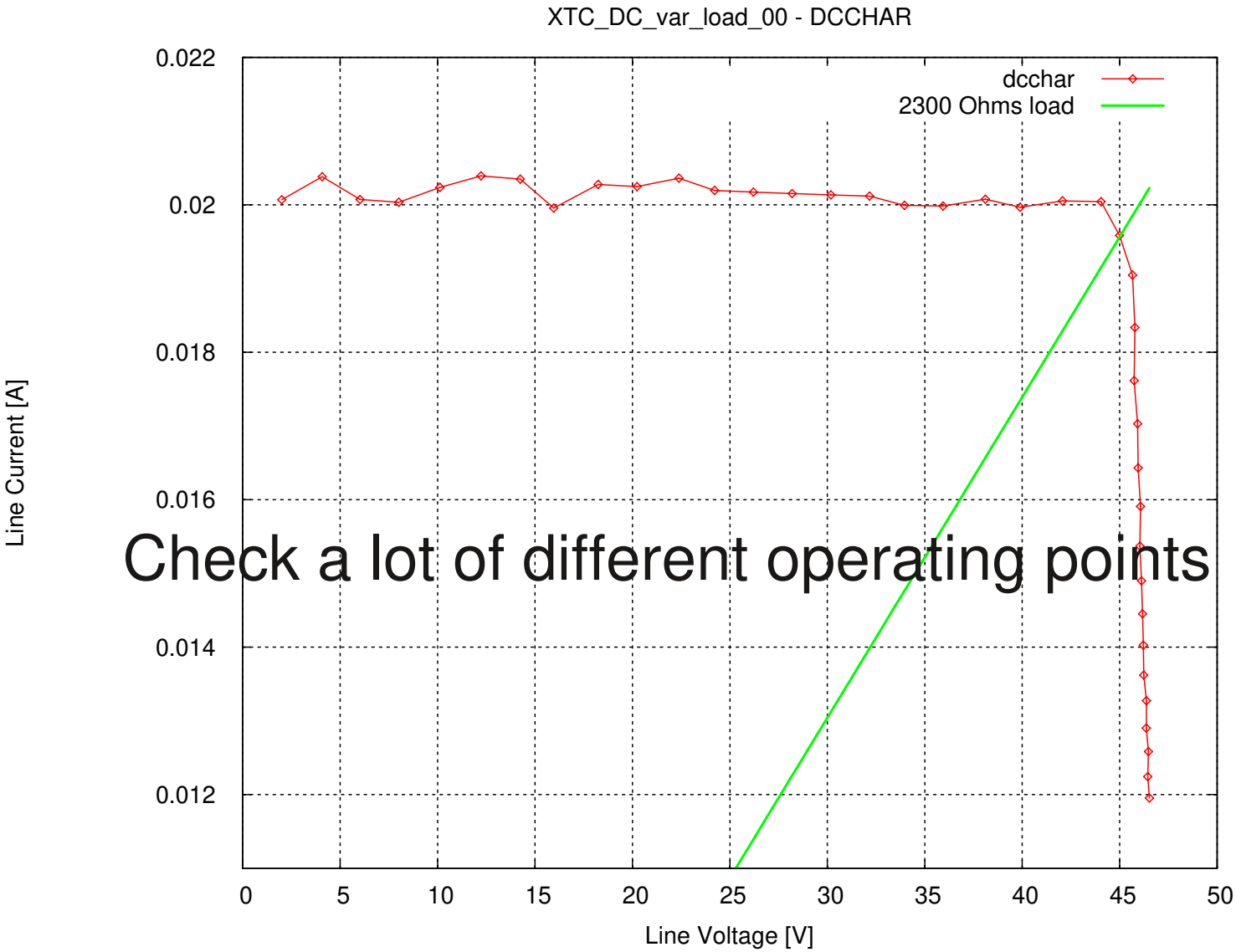
SystemC model
(frequency and time domain)

Connecting modules together
Netlists
Testbenches

Adobe FrameMaker 7.1

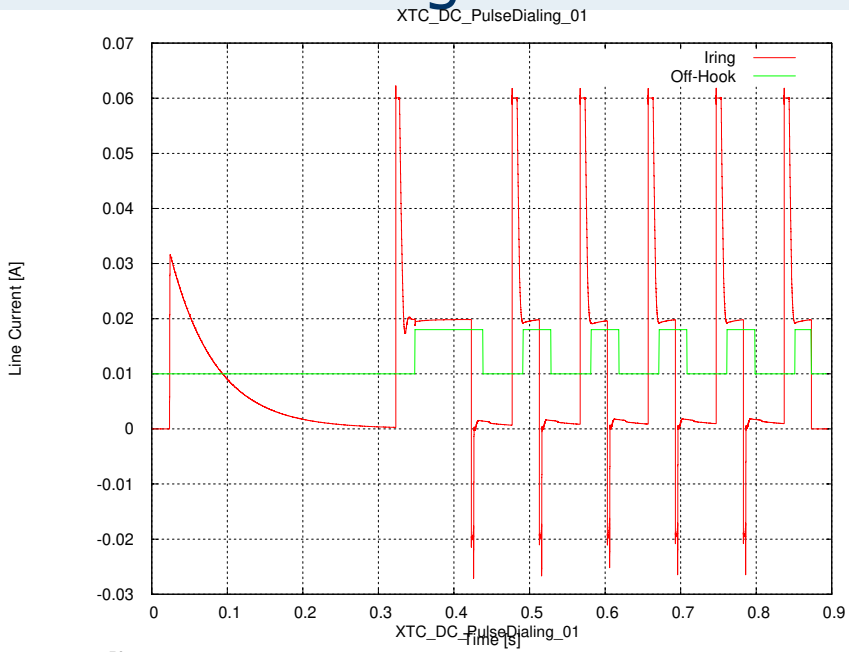
Documentation

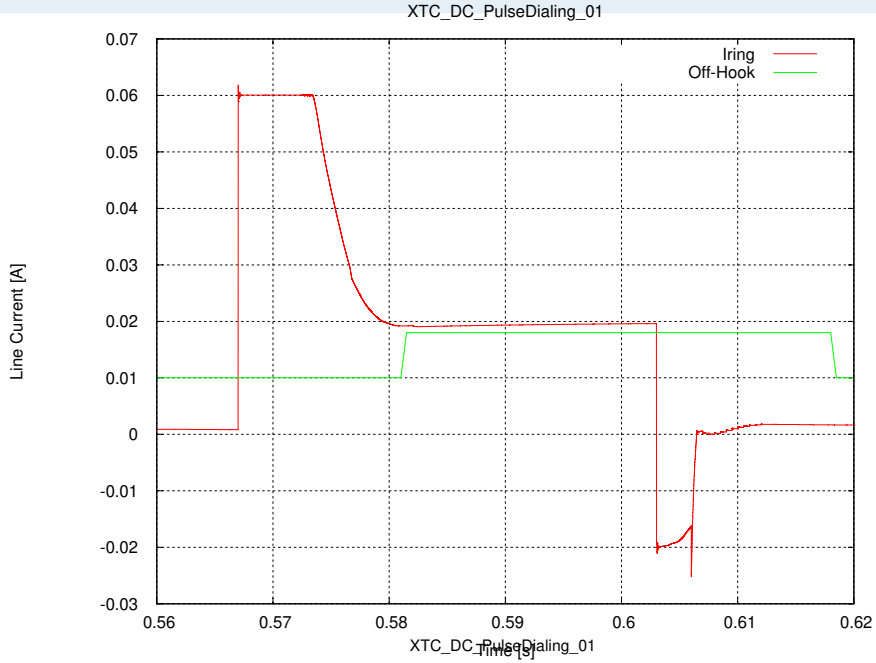
Some Simulation Results: DC Characteristic Simulation

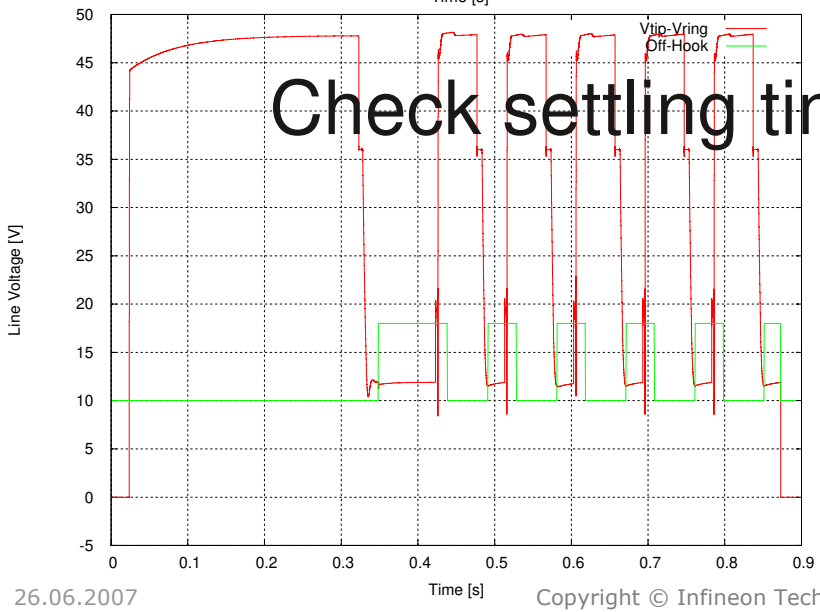


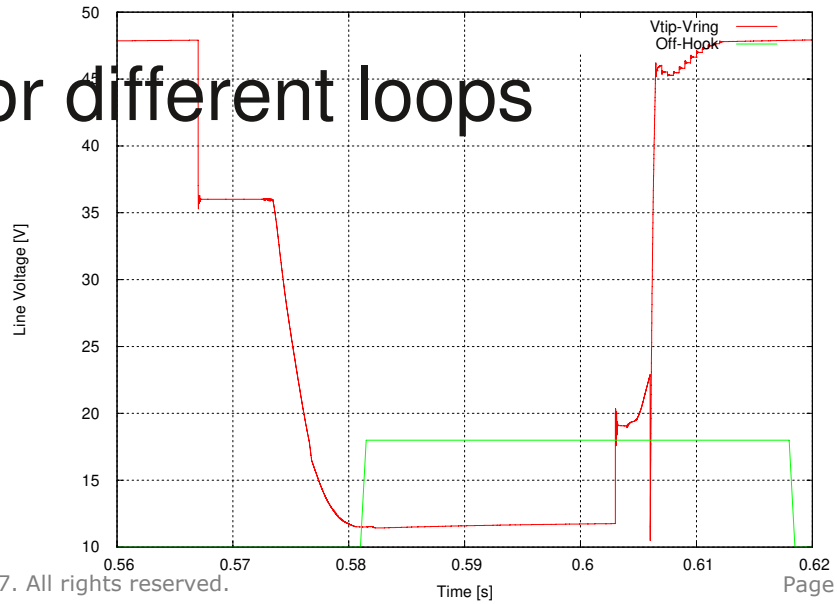
Check a lot of different operating points

Pulse Dialing Simulation



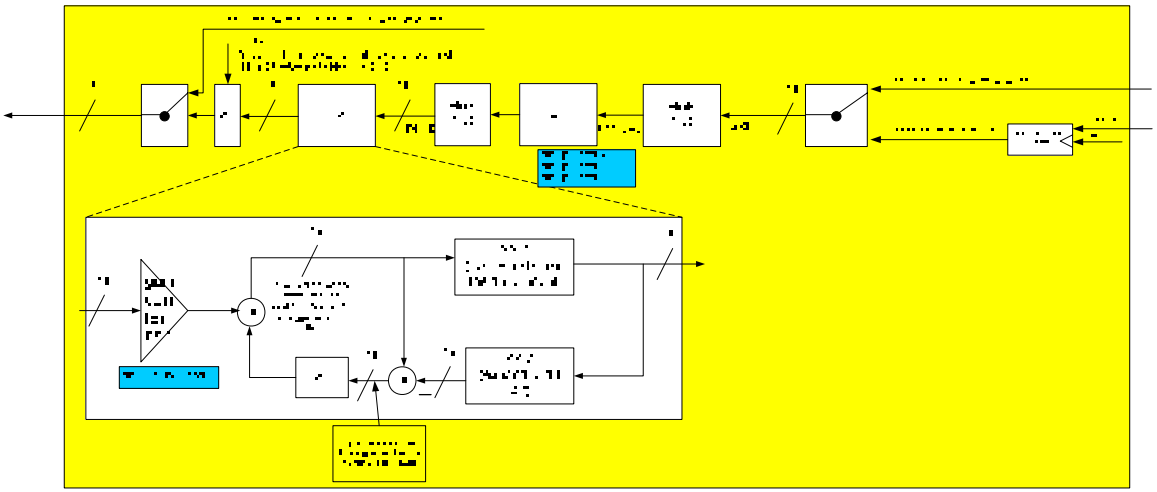




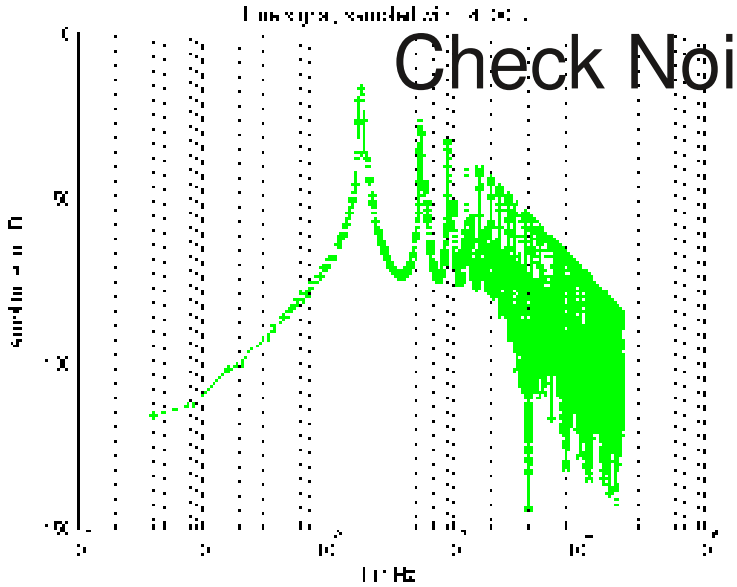


Check settling time for different loops

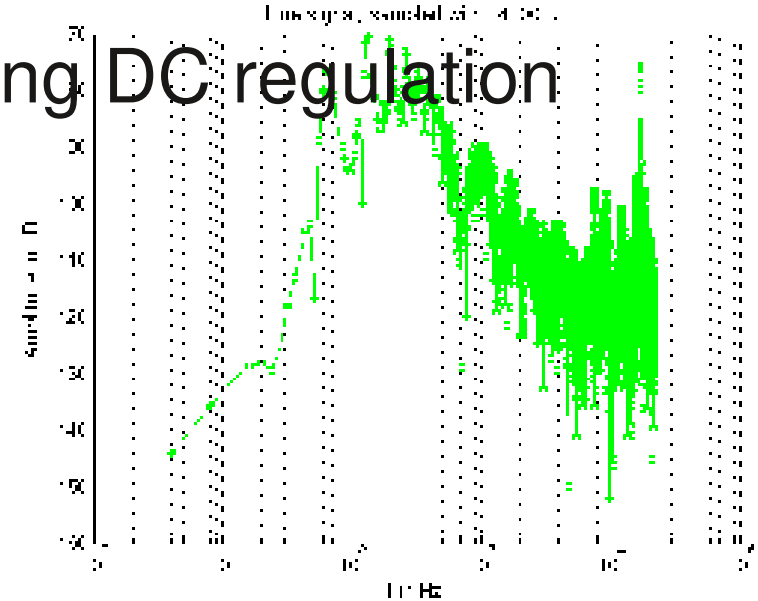
DC Regulation Noise



Check Noise during DC regulation



without noise shaper



with noise shaper

Thank you …

Never do a complex system without system simulation

Never stop thinking