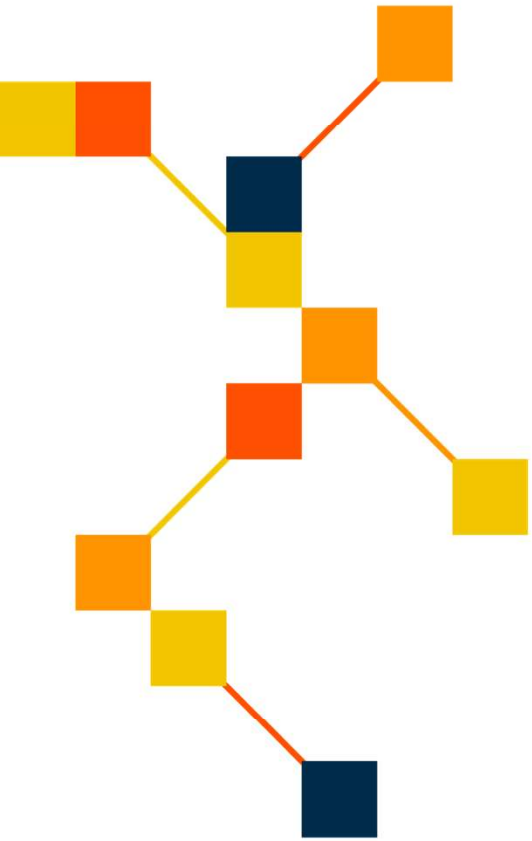


Arteris TLM models for performance analysis

Rocco Jonack, Principle Corporate Application Engineer
Jean-Blaise Pierres, Senior Manager Partner Ecosystem

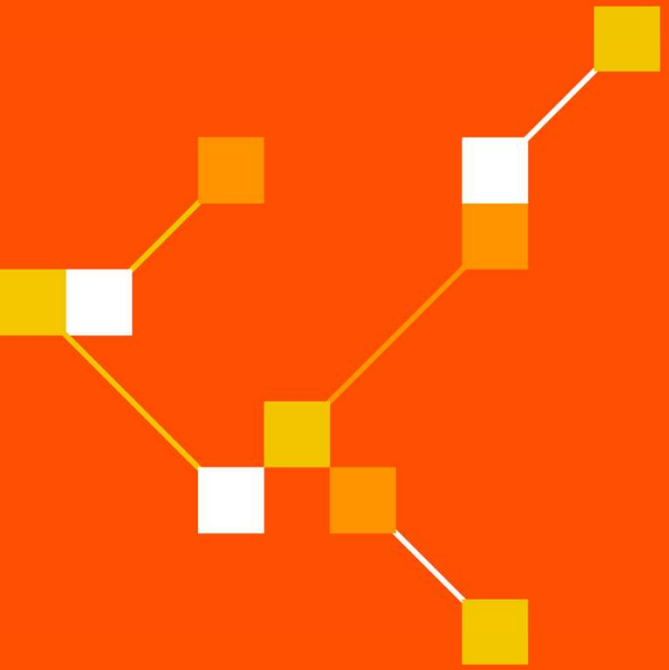
ARTERIS IP

1 Arteris Company Overview

2 Arteris Ecosystem

3 Arteris Technology Overview

4 Usage of models in performance analysis



Arteris Company Overview

Connecting Innovation

Arteris – A Leading SoC System IP Company & NoC Pioneer

Global customer base deploying Arteris interconnect IP and SoC integration software

- Silicon-proven IP used in **over 3.85 billion**+ units shipped to date[1]
- **880+ SoC design starts** to date[1]
- **70-80%** market share of **automotive ADAS** SoC market[2]
- Strong technology and traction in **AI/ML systems**
- **Ecosystem** - any processor, any IP, any EDA, any foundry
- Customer **retention rate of 90+%**[1]
- 108 patents and 137 patent applications[3]
- **ISO 9001**:2015 Quality Management System (QMS) Certified
- **ISO 26262** Certified for Automotive Functional Safety for Magillem software and Ncore coherent interconnect IP

[1] Over a three year period ending June 30,2025
[2] Management estimates
[3] As of June 30, 2025

Diversified Customer Base

Subset of Publicly Disclosed Customers

Seasoned Executive Team With Deep Domain Expertise

Charlie Janac

Chairman, President and Chief Executive Officer

Paul Alpern

EVP, Chief Legal Officer and Corporate Secretary

Jolene Bishop

EVP and Chief Human Resources Officer

Nick Hawkins

EVP and Chief Finance Officer

Laurent Moll

EVP Engineering and Chief Operating Officer

Michal Siwinski

EVP, Chief Product Officer and Chief Marketing Officer

Ken Way

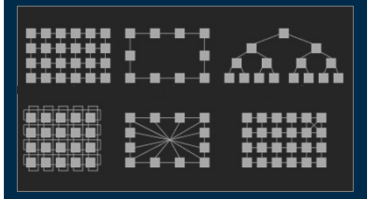
EVP Sales and Chief Customer Officer

cadence
Brooks
MACOM
MIPS
WAVE COMPUTING
Qualcomm
CORSAIR
pwc
Qualcomm
NVIDIA
cadence
Mentor A Siemens Business
XILINX
freescale semiconductor

Arteris – Addresses Emerging Trends in Electronics

Growing design complexity, tightening performance constraints and lack of NoC expertise compound time-to-revenue challenges

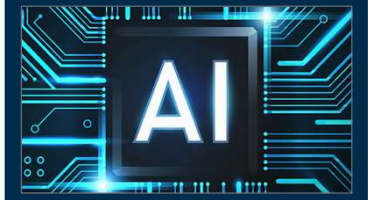
Accelerating Complexity



More Processors & IP Blocks Data movement key competency 'Data movement and storage operations can account for up to 84% of the dynamic energy usage of a GPU's system-on-chip (SoC)*.'

Source: HAL open science paper, Jun'24

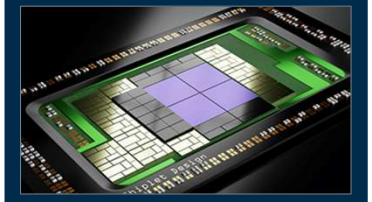
Artificial Intelligence



By 2030, the total generative AI compute will serve 70 percent of business-to-consumer and 30 percent of business-to-business applications **.'

**Source: McKinsey, Mar'24*

Chiplets



'Multi-die systems have emerged as the solution to go beyond Moore's law and address the challenges of systemic complexity***.'

***Source: Semiconductor Engineering Oct'23*

OEMs Going Vertical

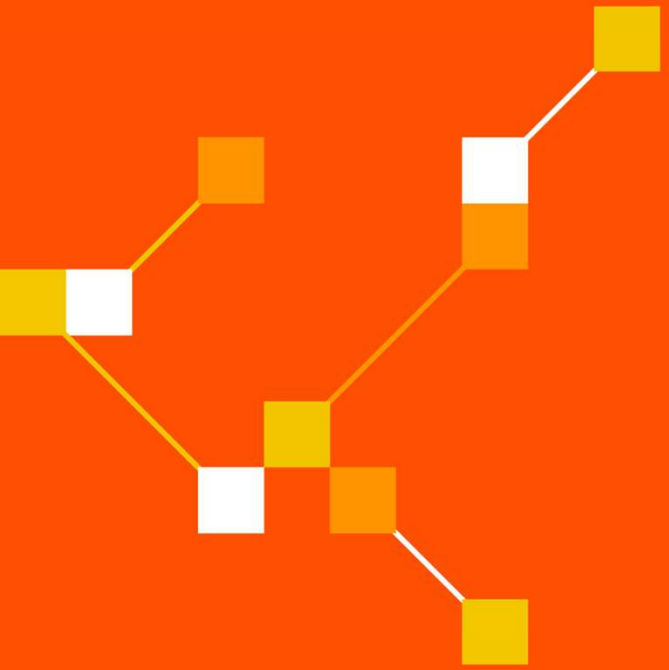
'OEMs are increasingly embracing vertical integration in their design practices, including implementing their own SoCs.****.'

****Source: Synopsys Feb'22*

Robotics

'Humans are set to interact with polyfunctional robots at an increasing rate: 80% of us will use them on a daily basis by 2030, up from 10% today*****.'

*****Source: Forbes Oct `24*

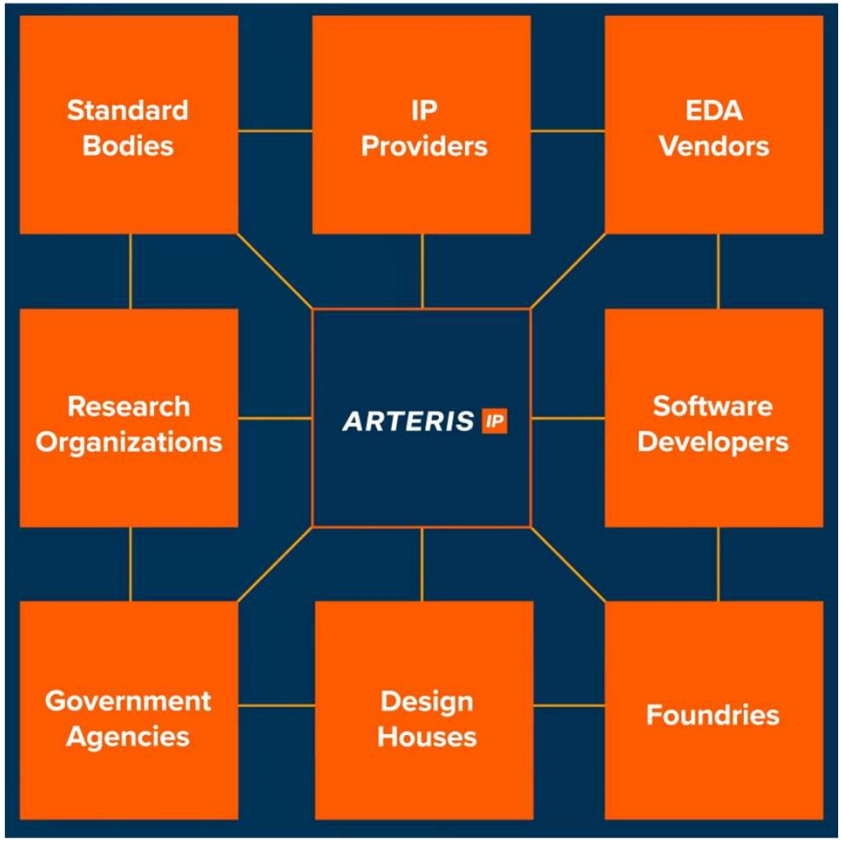


Arteris Ecosystem

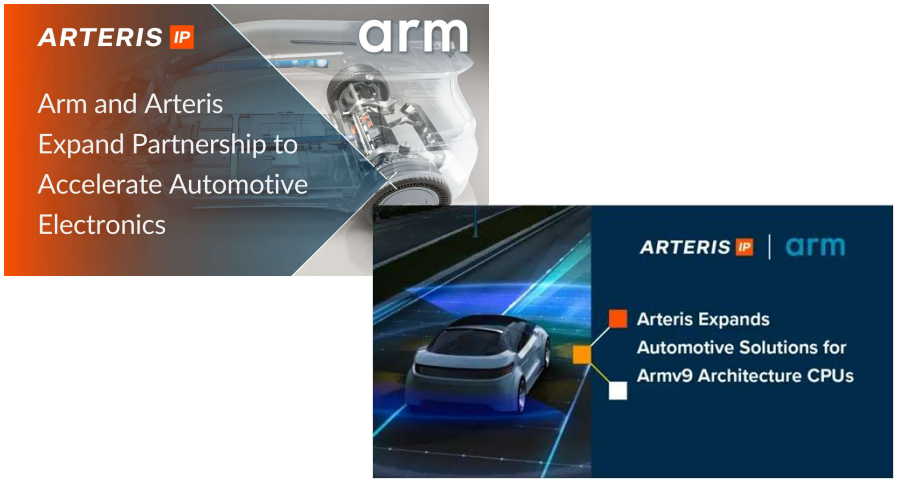
Overview

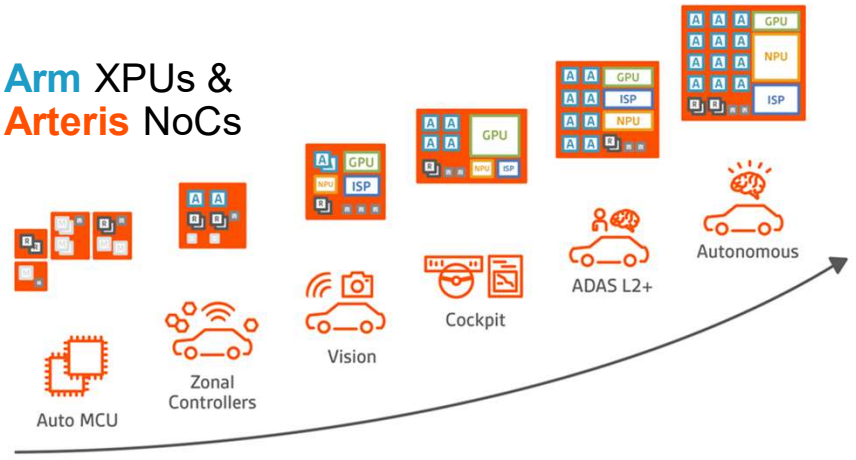
Connected With Arteris

Arteris' technology is **agnostic** and connects across the **semiconductor ecosystem**, easing and derisking designs



Arteris and Arm Collaboration on IP, MCUs, Chiplets, and SoCs



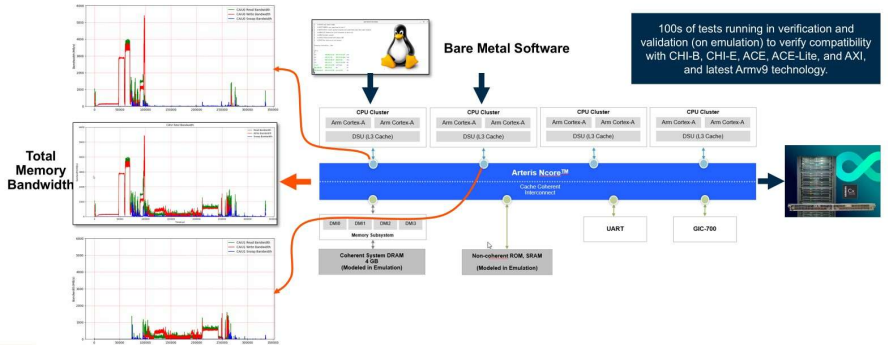


Pre-Validation Tests **Ensure Trust in Arm + Arteris Connections**
Ecosystem integration with Arm – running on emulation

We are at an inflection point in the automotive industry that requires a fundamental rethink of automotive product development and deployment methodologies. The latest generation of Arm Automotive Enhanced compute and software solutions, integrated with Arteris' flexible and configurable Ncore cache coherent interconnect IP, means customers can begin development sooner, accelerating time to market for next-generation vehicle electronics.

arm

Suraj Gajendra, vice president of products and solutions, Automotive Line of Business, Arm

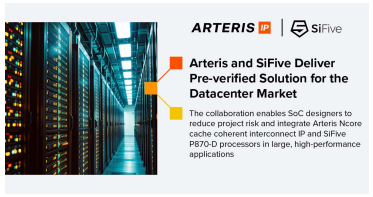


Sources: Arm, Arteris, D&R, Semiengineering
ARTERIS IP

Arteris and RISC-V Ecosystem Collaboration and Interoperability

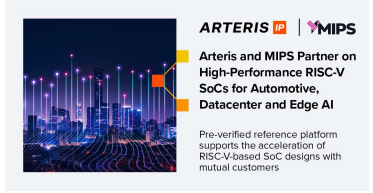
Broad and Expanding Ecosystem

SiFive



ANDES TECHNOLOGY

MIPS



semidynamics

SYNOPSYS®

達摩院 | XUANTIE

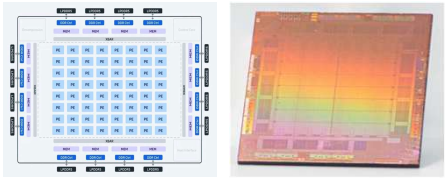
Silicon-Proven Examples

mobileye + MIPS

Mobileye EyeQ ULTRA
with MIPS eVocore P8700
L4 Autonomous Vehicle

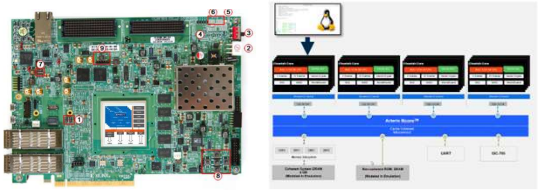
Meta + ANDES TECHNOLOGY

Meta MTIA v2
with Andes Technology QiLai
Large-Scale AI/ML



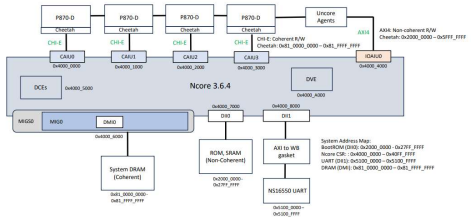
Tested Interoperability

Test Boards, Simulation, and Emulation



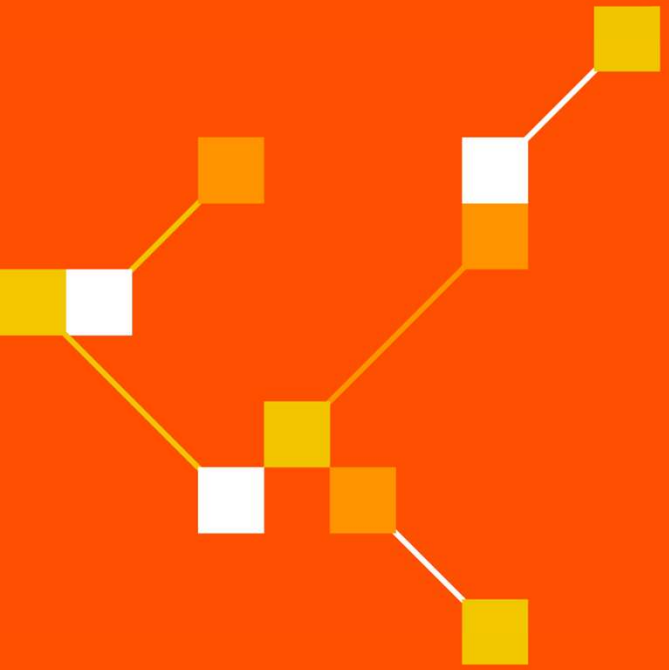
System Configurability

Software (Magillem) driven IP
Configurability of RISC-V CPUs and NoCs



Sources: SiFive, Andes, MIPS, Semidynamics, Synopsys, Damo Academy, Hot Chips, SMYG Limited

ARTERIS IP



Arteris Technology

Overview

Trusted Comprehensive Families

Non-Coherent Interconnect IP

FlexGen
FlexNoC
FlexWay
+ Size Options
+ Safety Options
+ Reliability Options

CodaCache

Last-Level Cache IP

Coherent Interconnect IP

Ncore

+ Size Options
+ Safety Options
+ Multi-Die Options

SoC Integration SW

Magillem Registers
HW/SW Interface

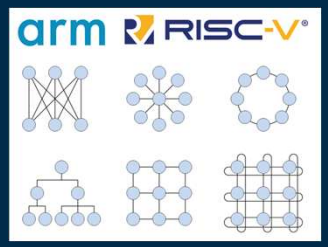
Magillem Packaging
IP Packaging

Magillem Connectivity
IP & SoC Assembly

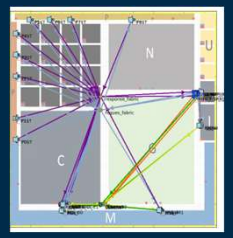
FlexGen Capabilities with 80+ Patent Properties/Applications Filed

Smart NoC IP technology based on years of experience and solid technology foundation

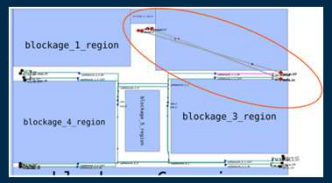
Processor and topology agnostic



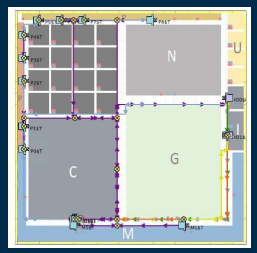
Automated and manual editing at major stages



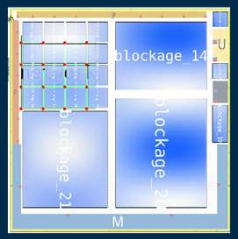
Incremental design capability



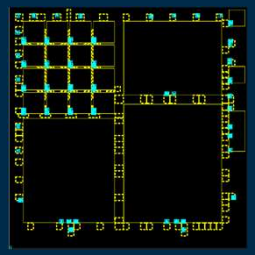
Comparable QoR to manual generated NoC



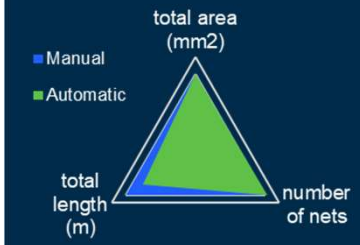
Robust floorplan input and output



P&R begins earlier and finishes earlier



Optimization for wires, performance, area



Fast and high capacity NoC connectivity

Topology Generation:
FlexGen 4hrs vs 20hrs

Initial Optimization:
FlexGen 10mins vs 3hrs

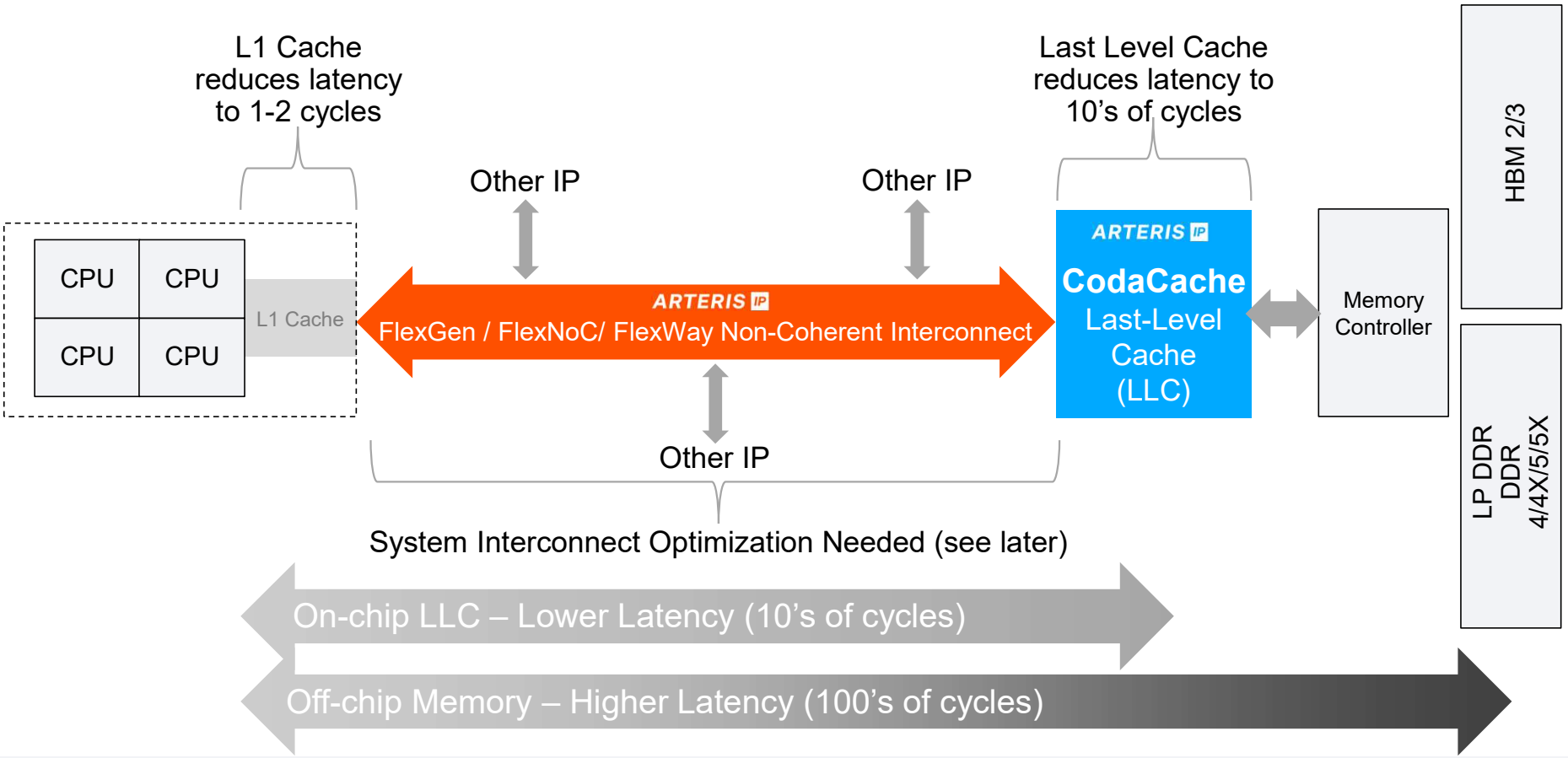
Final Optimization:
FlexGen 100min vs 2wks

Many Iterations → Few

ARTERIS IP

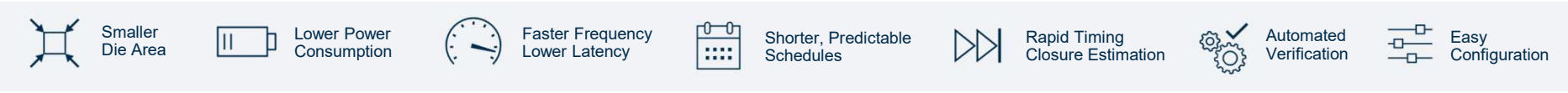
Maintaining CPU performance using Non-Coherent caches

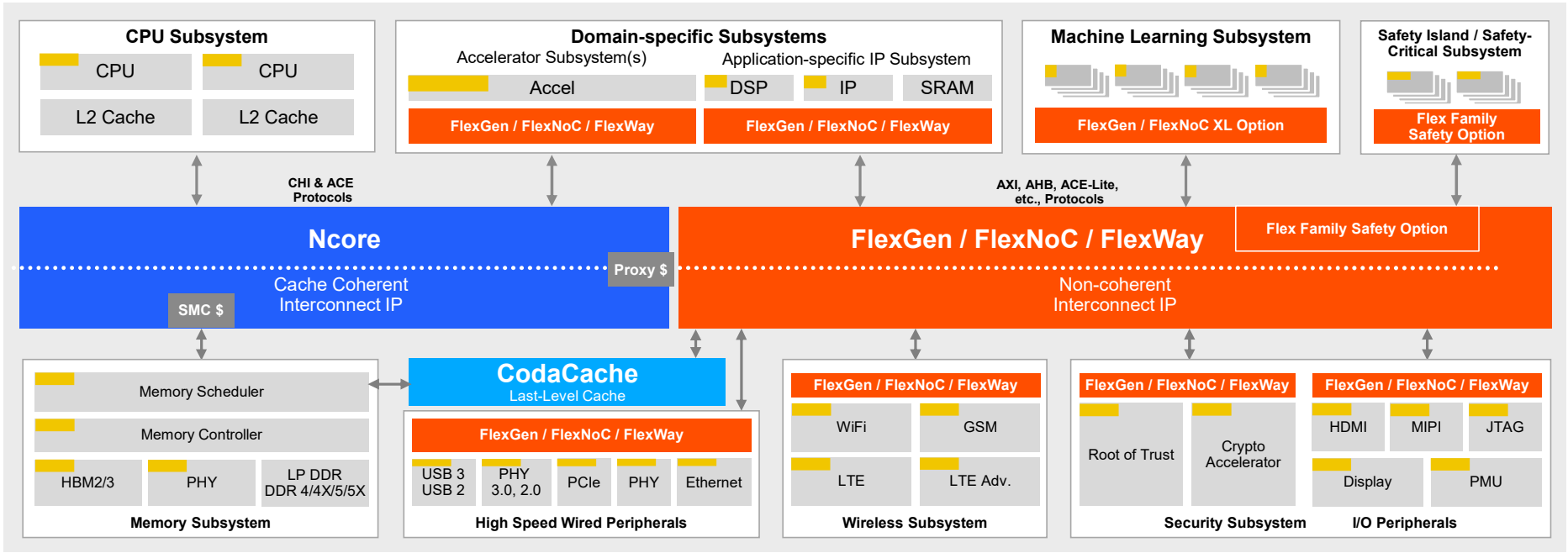
CPU performance depends on compute capability and data availability



One-Die System IP and Network-on-Chip (NoC) SoC Interconnect IPs

Networking techniques for improved on-chip communication & data flow





Arteris Ncore™
Cache coherent interconnect IP

Arteris FlexGen™, FlexNoC®, FlexWay™
Non-coherent interconnect IP

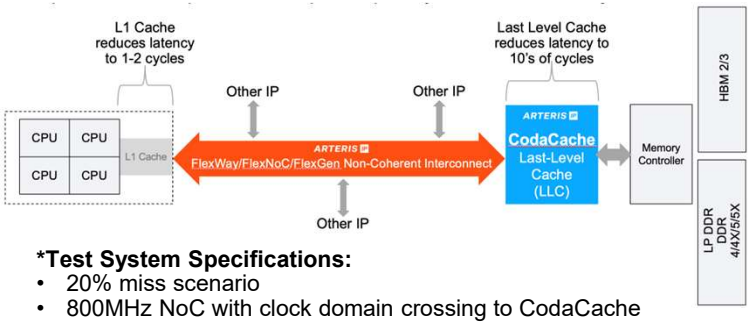
Arteris CodaCache®
Last-level cache IP

Arteris Magillem® Registers
Hardware/Software interface

CodaCache

Last Level and/or Dedicated Cache Controller Complementing FlexGen / FlexNoC / FlexWay IP

- Reduces system latency with higher hit rates.
- Boosts bandwidth in high-traffic systems.
- Power savings through fewer memory transfers.



***Test System Specifications:**

- 20% miss scenario
- 800MHz NoC with clock domain crossing to CodaCache
- CodaCache at 1.5GHz
- DDR-1600

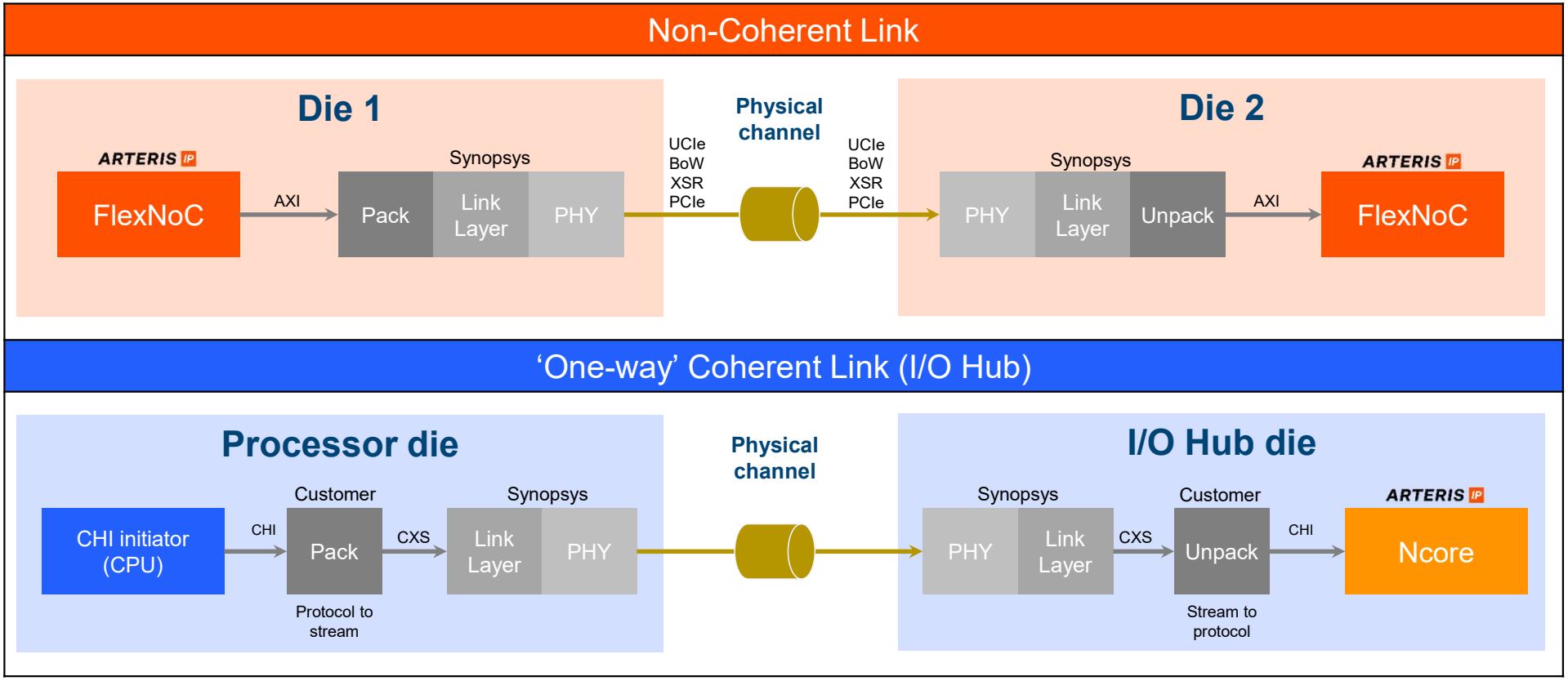
For a CodaCache with data width=16B and cacheline size=64B.
All read accesses.

*Sample Test System	Bandwidth GB/s	Average Latency Cycles	Latency Minimum Cycles	Latency Maximum Cycles
Without CodaCache	12.5	300	28	406
With CodaCache	23.4	36	30	147
Relative Gains	+87%	8.3X	+6.7%	-64%

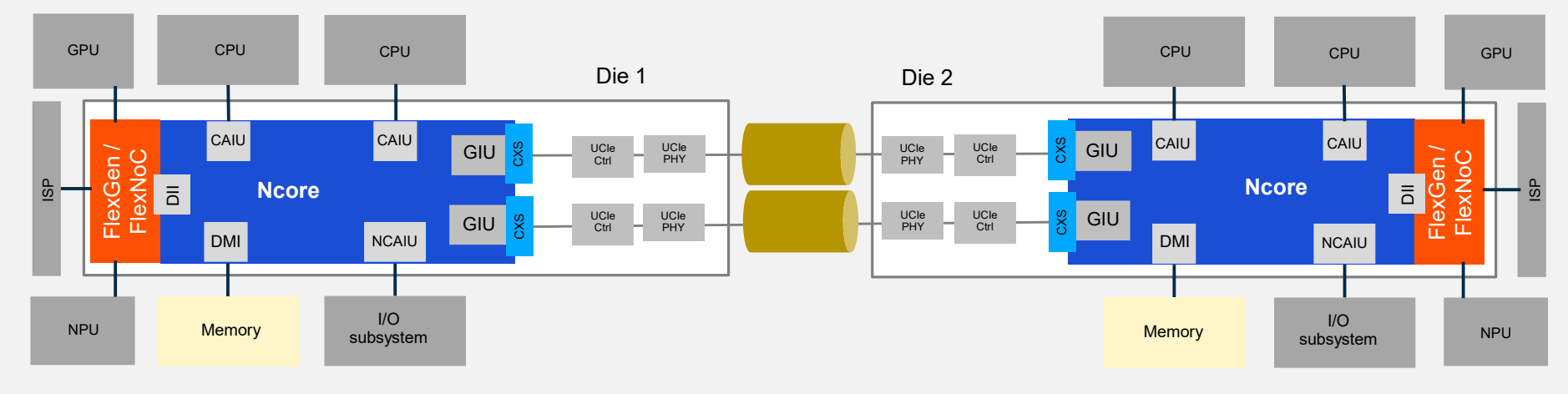
Enables SoC Developers to Improve SoC Performance by 50-60%

ARTERIS IP

Silicon Proven Arteris Multi-Die Solution Baseline

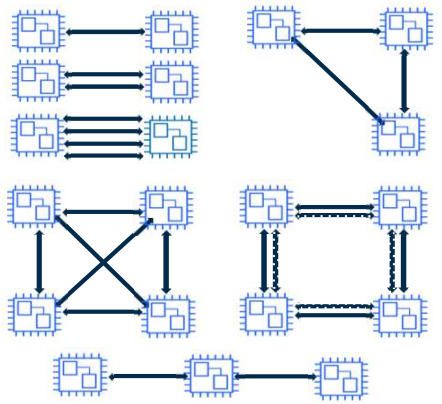


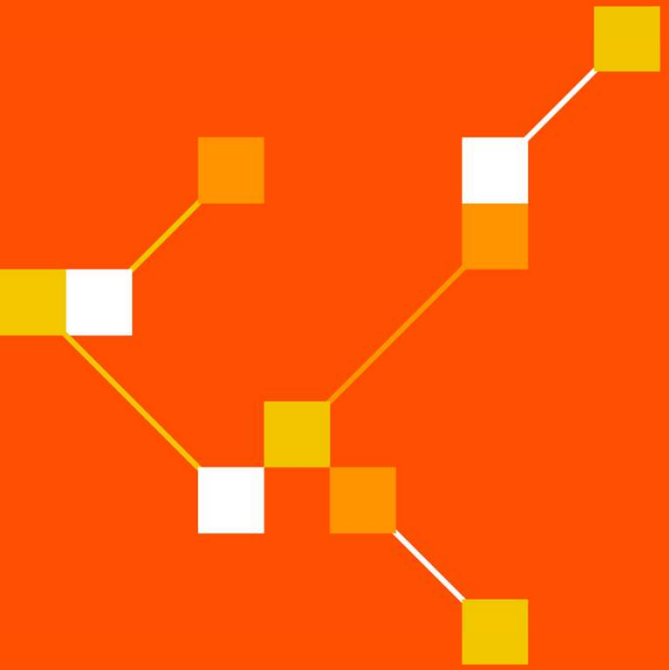
Arteris Expanded Multi-Die with Fully-Coherent End-to-End Scaling



Advantages

- High-performance interface to distribute NoCs seamlessly across chiplets
  - Low-latency Ncore-to-Ncore coherent die-2-die communication
  - Gateway Interface Unit (GIU) tunnels Arteris protocol to GIU on other die
- Supports industry standards
  - UCIe, PCIe, and Arm AMBA support
  - Arteris Ncore coherent protocol over AMBA CXS PHY-independent packet streaming interface

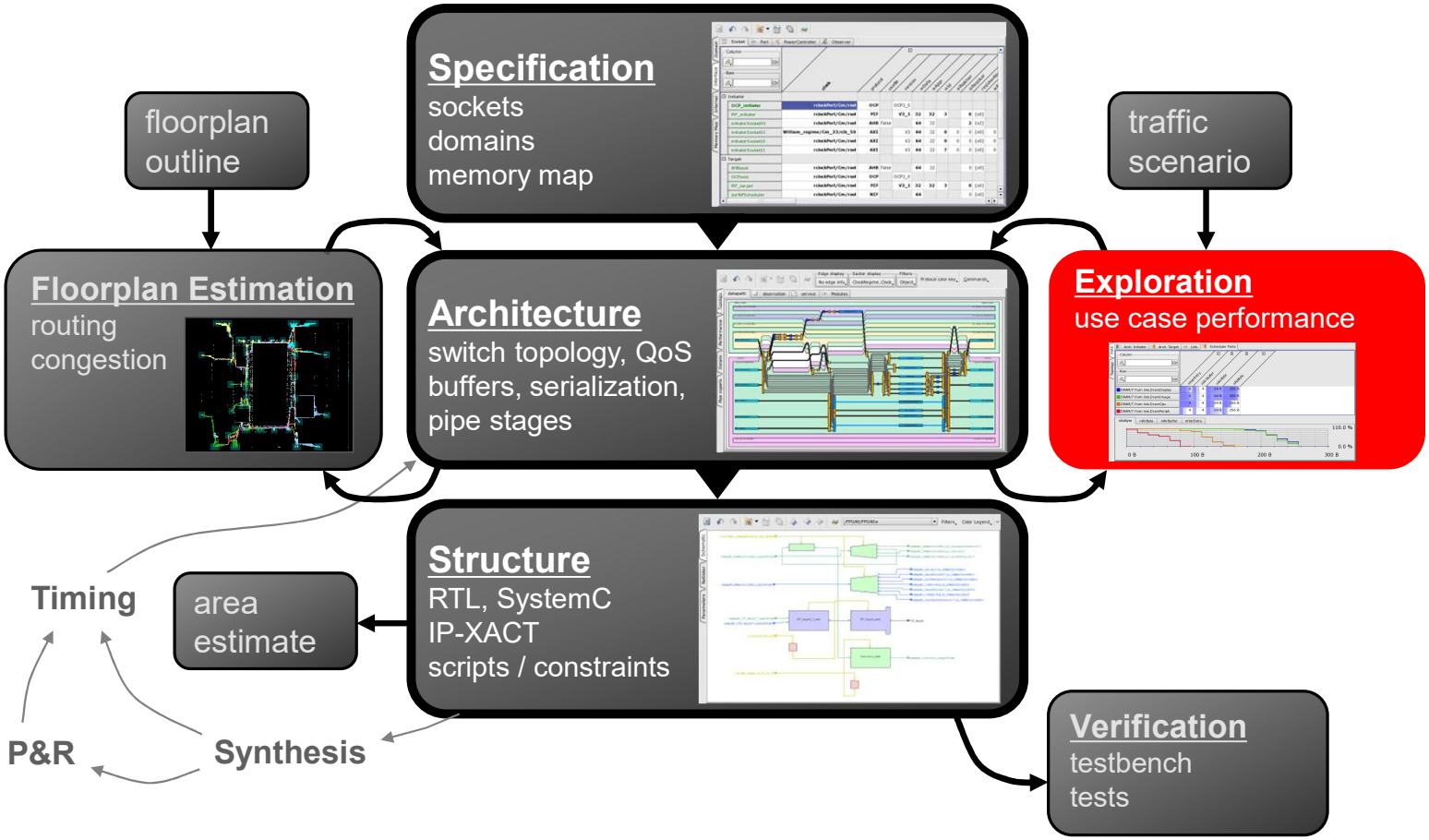




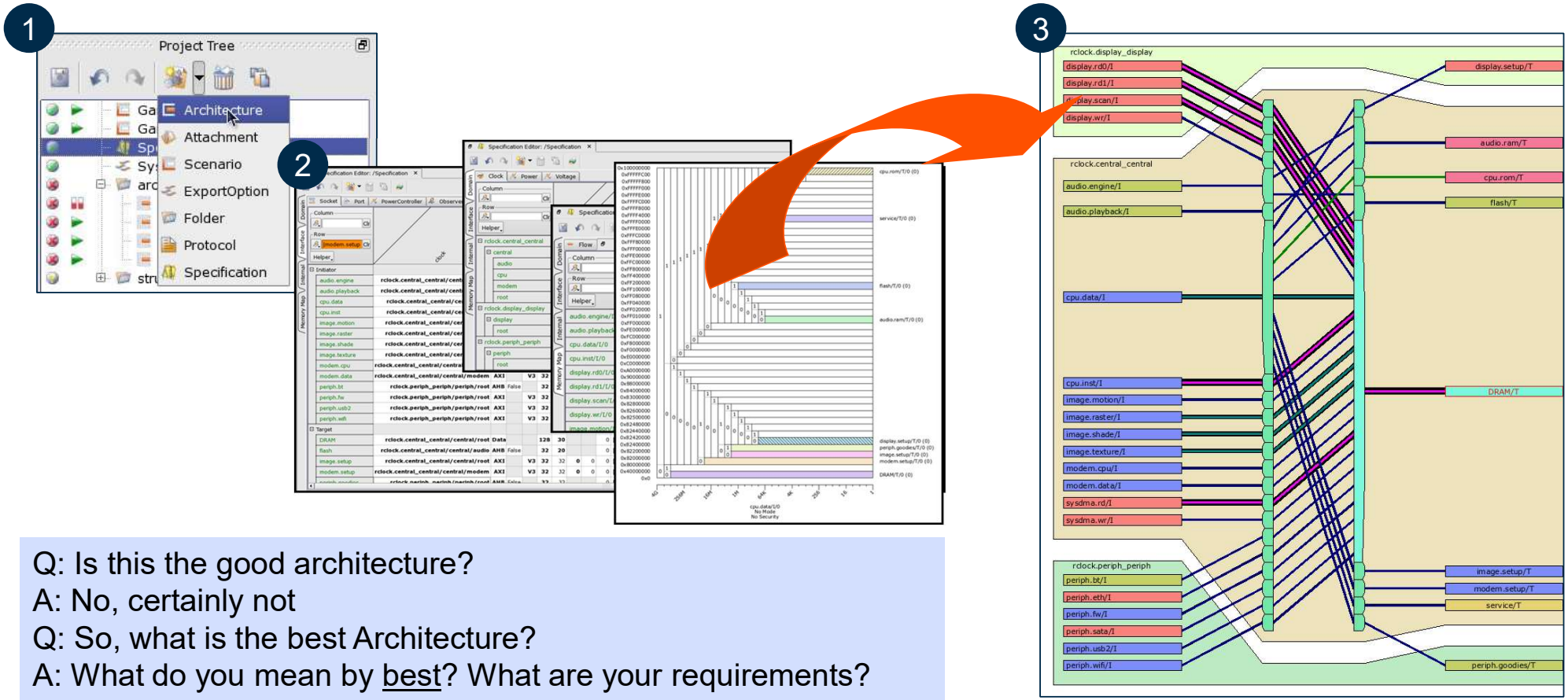
Usage of models in performance analysis

Overview

Tool Flow for NoCs



Specification to Architecture Generation

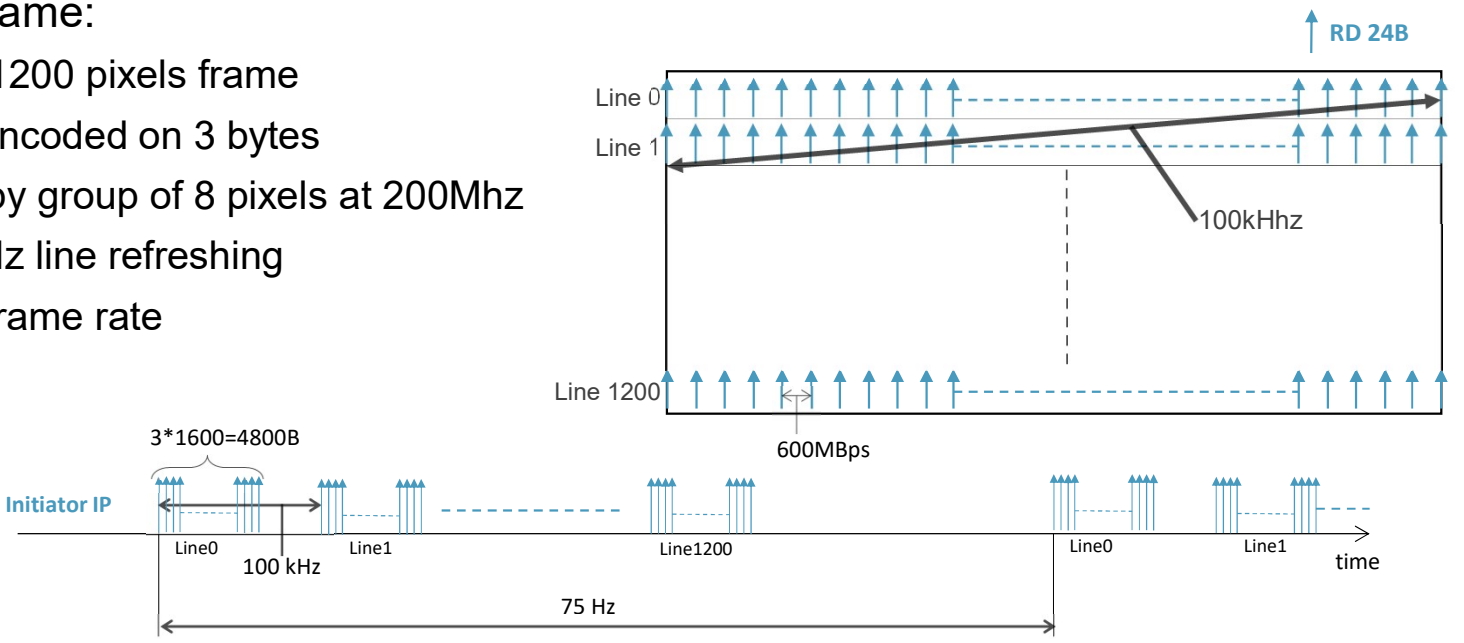


Q: Is this the good architecture?
A: No, certainly not
Q: So, what is the best Architecture?
A: What do you mean by best? What are your requirements?

ARTERIS IP

Performance Goal Definition Example

- Video Frame:
  - 1600x1200 pixels frame
  - Pixel encoded on 3 bytes
  - Read by group of 8 pixels at 200Mhz
  - 100 kHz line refreshing
  - 75Hz frame rate



*Procedure = (((((Read(24) / 600 ** MBps)*4800 ** B) / 10** us) * 1200) / 13.33 ** ms) (rasterAddrGen)>> queue*

200Mhz 3Bytes per pixel — 1600px line — 100Khz vertical jump — 1200 lines — 75Hz frame rate

ARTERIS IP

Process Satisfaction & Target Usage

- Self Checking Testbench
- Scenario also defines real time constraints
- Allow verifying the achieved QoS

Scenario result: /import.GamingQos_architecture.step1_1e_4.000.ScenarioResult

Process | Queue | Scen. Initiator | Scen. Target | Target Model

Column Clr
Row Clr
Helper

	Required Efficiency	Efficiency	Satisfaction	Throughput	State
Process_CPU0	0.0 %	27.1 %	PASS	74.56 MB/s	
Process_CPU1	0.0 %	26.5 %	PASS	72.64 MB/s	
Process_CPU2	0.0 %	25.2 %	PASS	70.08 MB/s	
Process_CPU3	0.0 %	28.0 %	PASS	69.12 MB/s	
Process_DispRd0	100.0 %	69.2 %	FAIL	222.7 MB/s	
Process_DispRd1	100.0 %	69.2 %	FAIL	222.7 MB/s	
Process_DispScan	100.0 %	100.0 %	PASS	80.64 MB/s	
Process_DispWr	100.0 %	100.0 %	PASS	320.6 MB/s	
Process_Eth	0.0 %	100.0 %	PASS	201 MB/s	
Process_Image	70.0 %	36.1 %	FAIL	819.2 MB/s	
Process_Modem_CPU	60.0 %	48.9 %	FAIL	53.12 MB/s	
Process_Modem_Data	100.0 %	42.6 %	FAIL	128 MB/s	
Process_Sata	0.0 %	41.0 %	PASS	92.16 MB/s	

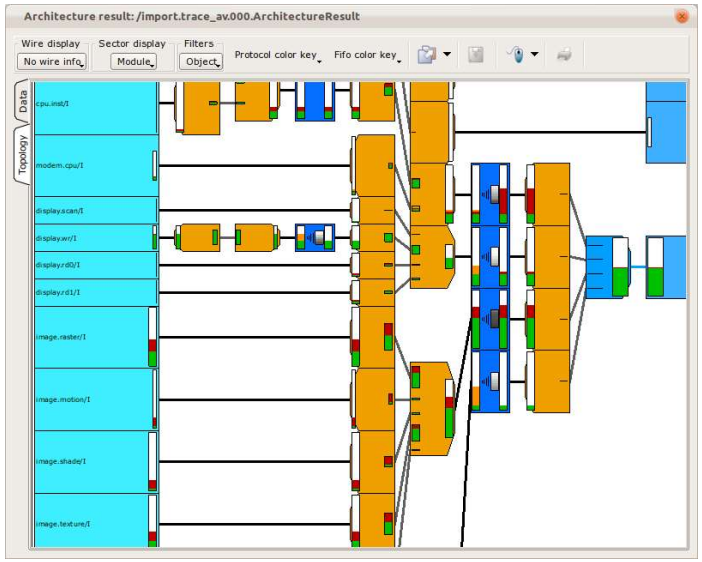
Process | Queue | Scen. Initiator | Scen. Target | Target Model

Column Clr
Row Clr
Helper

	Throughput	state	Read	Write	Busy	Wait	Throttle	Idle	Command Level	avg	max	Data Level
DramModel	1.957 GB/s		21.2 %	15.4 %	0.0 %	18.6 %	1.0 %	43.8 %	6	1.464	6	304 B

- Metric on the critical resource usage (DDR)

Performance Instrumentation View



Link States :

XFER/BUSY/WAIT/IDLE

width : word size

height : frequency

(area : peak throughput)

FIFOs :

Fill Level

width : word size

height : word count

(area : depth)

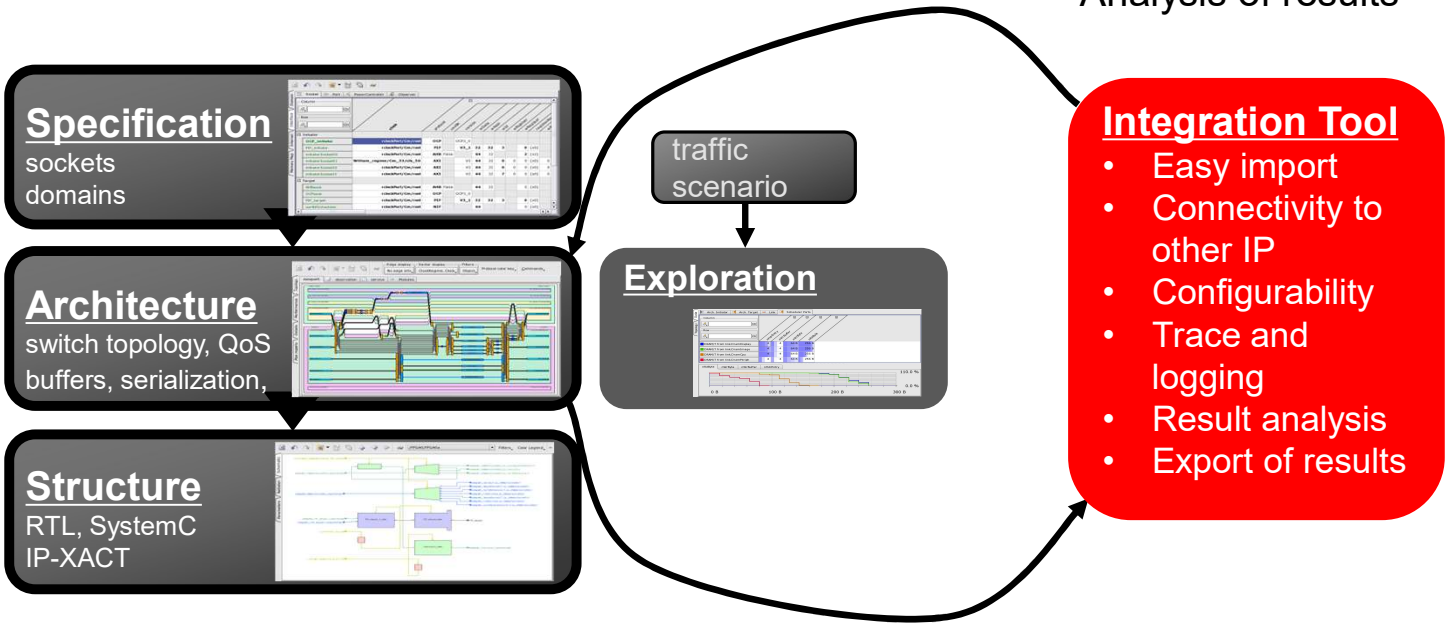
Much Used — Barely used

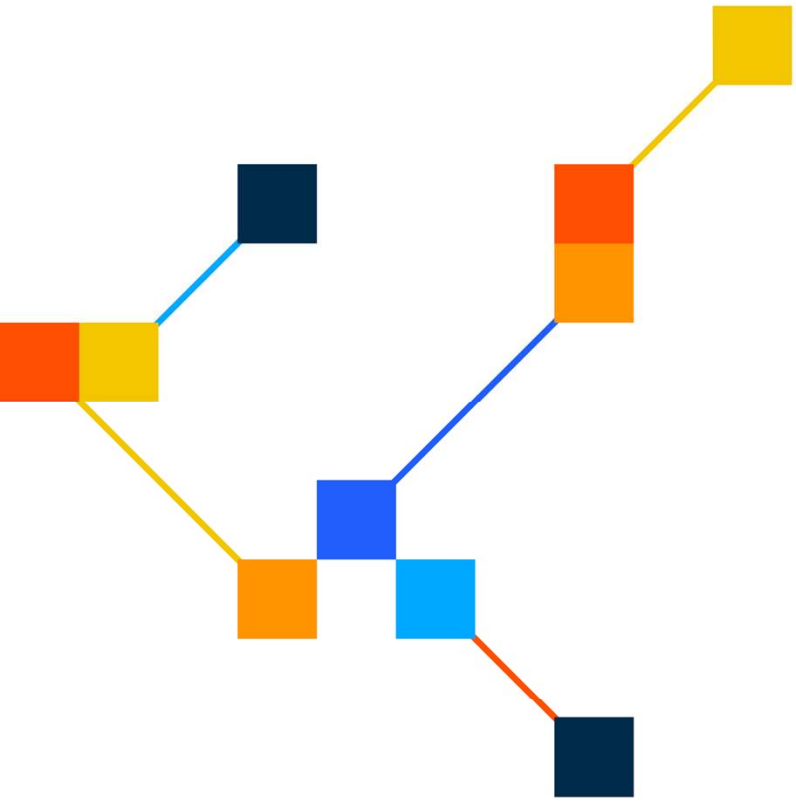
Model integration topics

- SoC contains many components
  - CPU subsystems for various purposes
  - Transaction latency is defined by interconnect and memory subsystem
  - Peripherals can define the specific SoC functionality
  - SW versus HW components
- Model simulations may have different purpose
  - VP models focus on SW, but require high speed
    - FlexNoC PV model
  - Architectural simulations require high cycle accuracy specifically for interconnect and memory components
    - FlexNoC AV model
  - Pin level models can substitute missing elements
    - FlexNoC VV model
- Integration tools come into the picture

Integration tools

- Tools support integration of various IPs
- Productivity of simulations
- Analysis of results





ARTERIS IP

Thank You