

MODELING THE AGC LOOP FOR DAB RADIO

PUBLIC

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SECURE CONNECTIONS
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AGENDA

- System Modeling with SystemC / -AMS
 - Use Case
 - System View
 - Subsystem View
- System Integration with IP-XACT
- System Simulation and Results

System Modeling with SystemC / -AMS



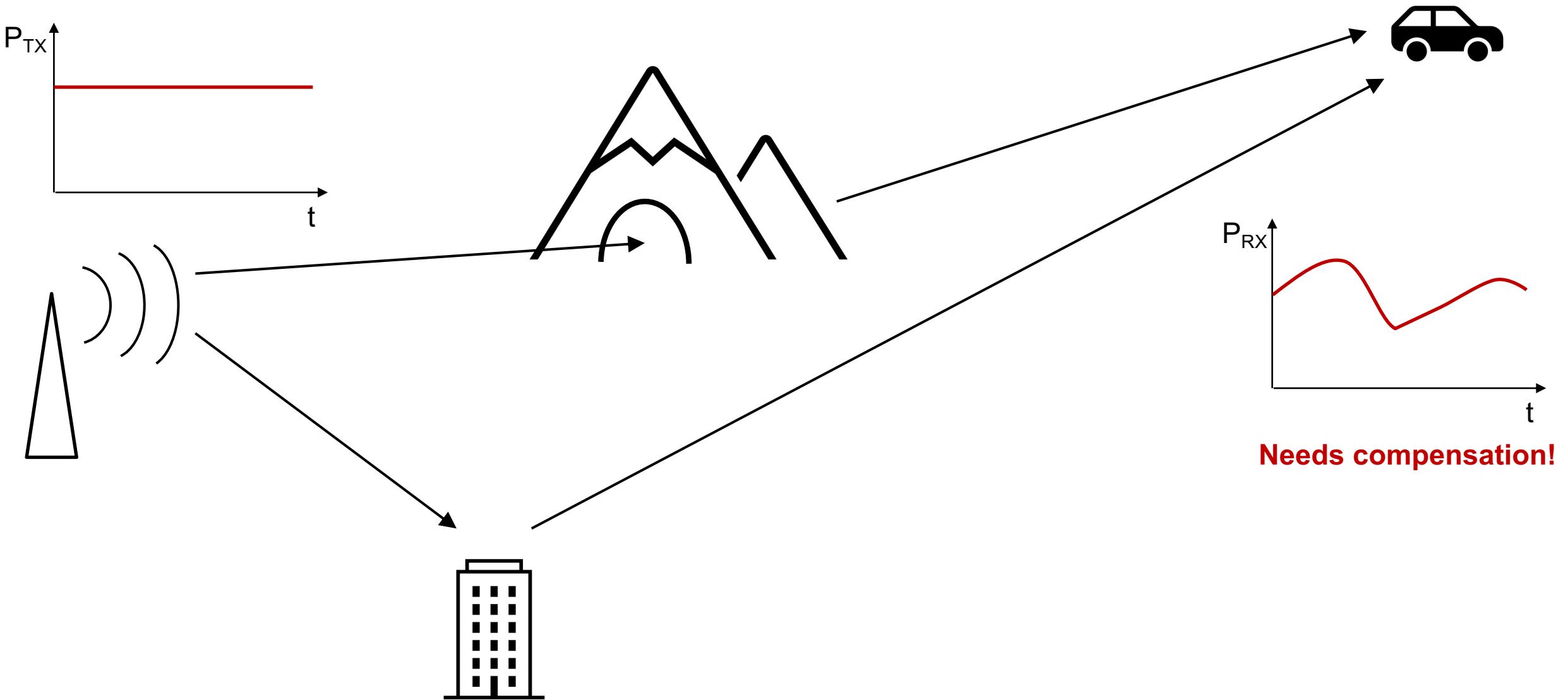
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USE CASE



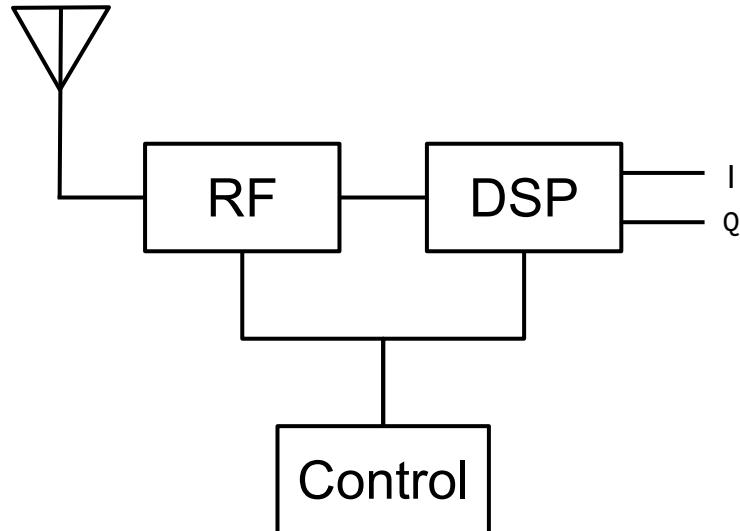
SYSTEM VIEW

1) Requirements

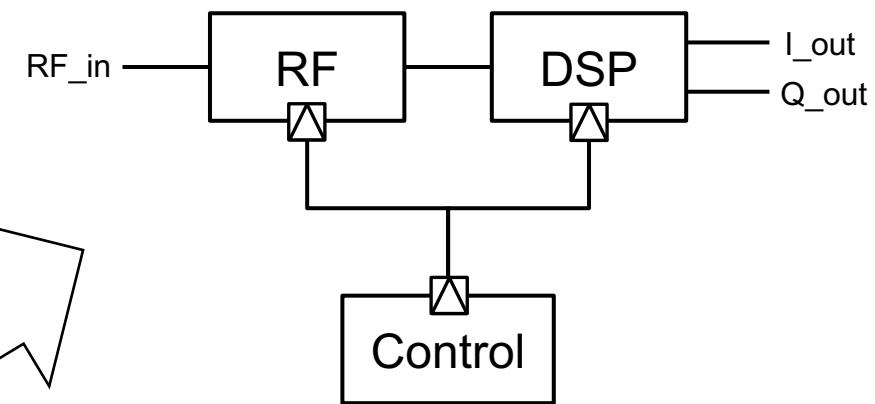
- Receive RF Signal
- Convert to Baseband
- Send Data Off-Chip



2) Map Functions to Subsystems



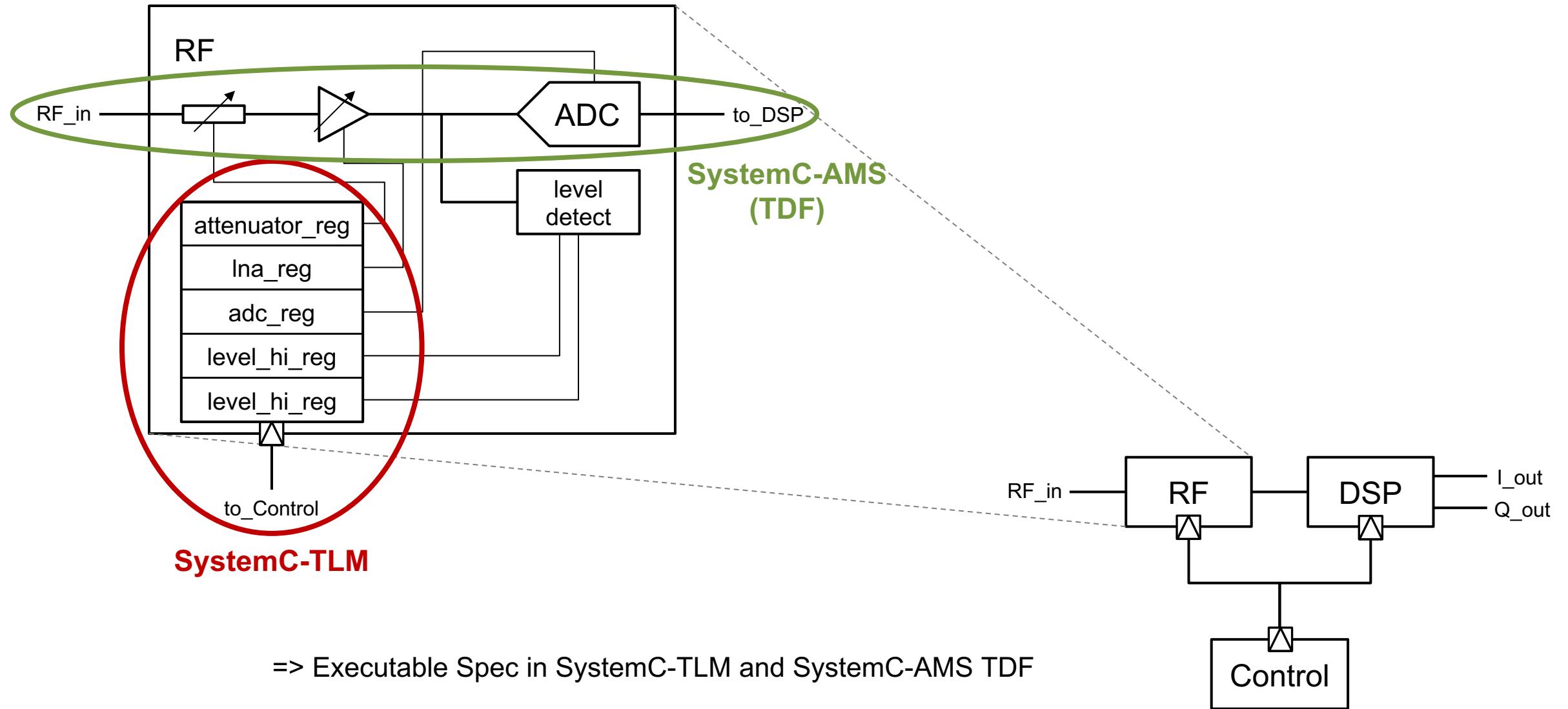
3) System Model



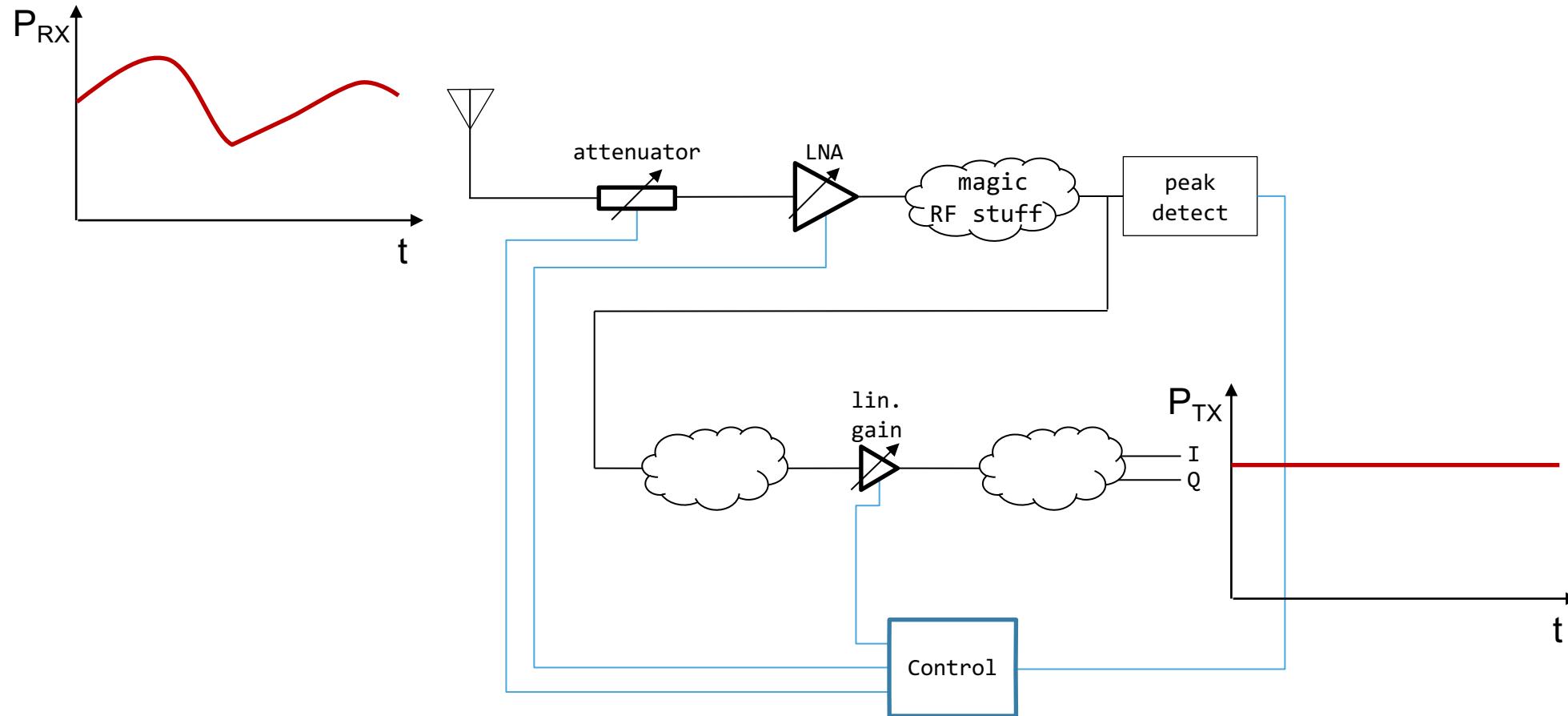
- Realistic Stimuli for Model V&V
- Block Interactions via Bus Messages
- Block Interface Standardization (Registers)

=> Executable Spec in SystemC-TLM

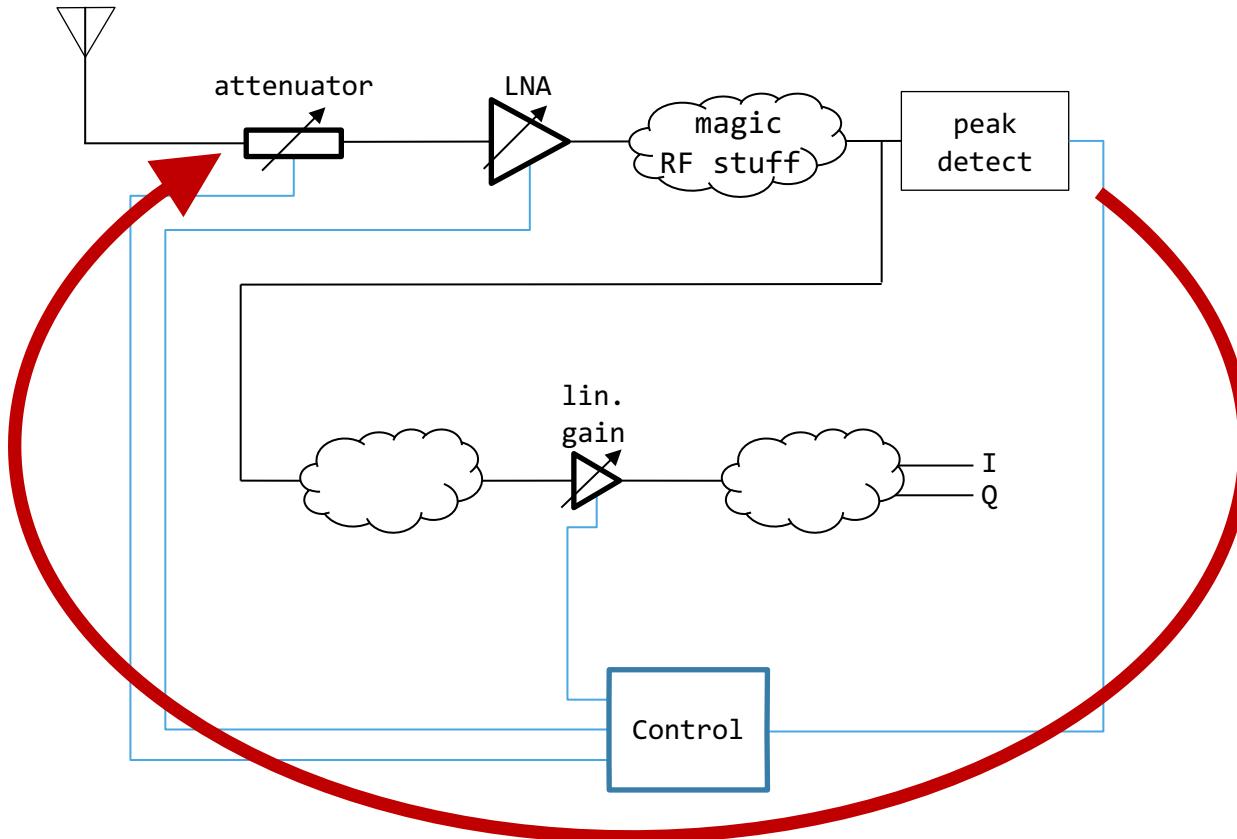
SUBSYSTEM VIEW



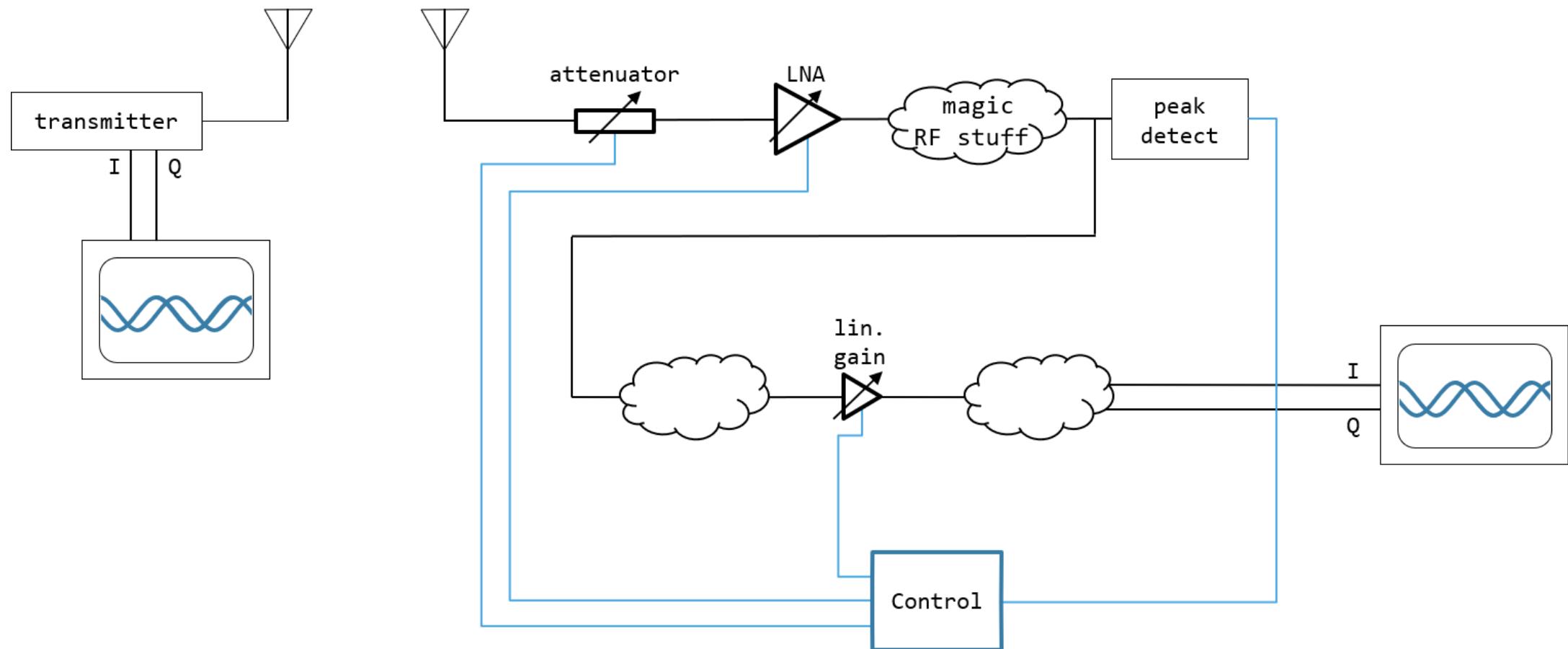
RF AGC LOOP



RF AGC LOOP



END-TO-END MODEL AND TESTBENCH



System Integration with IP-XACT



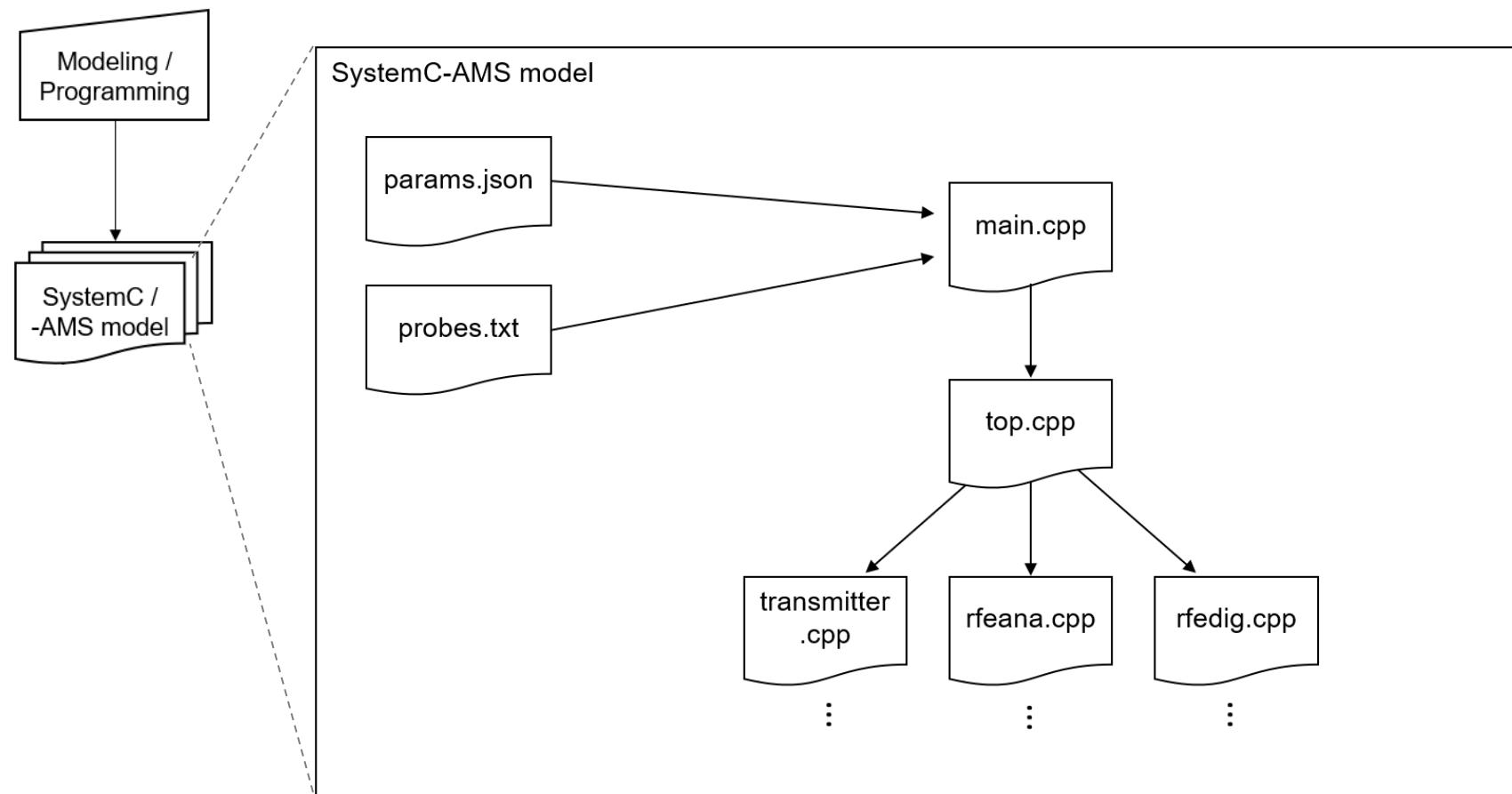
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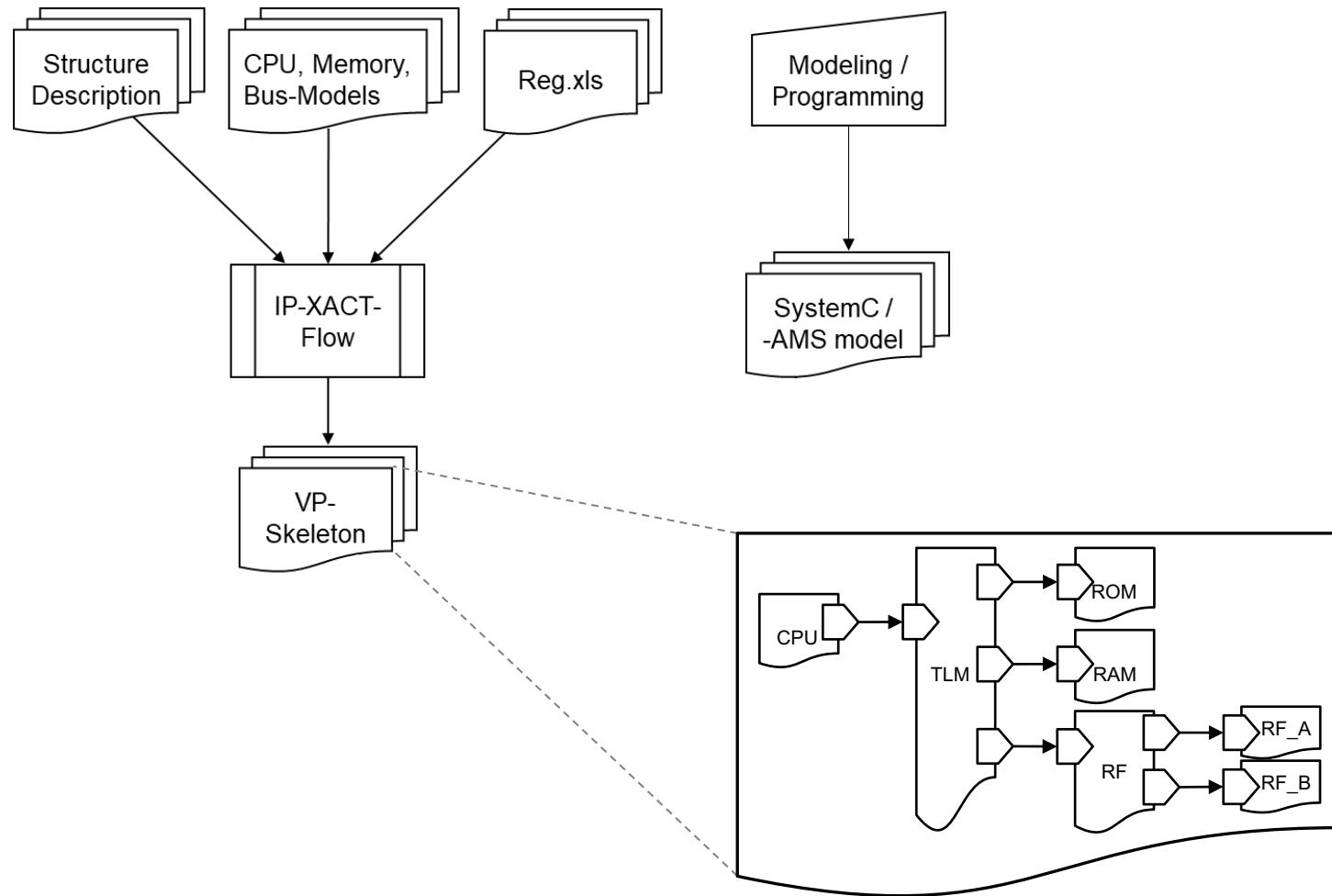
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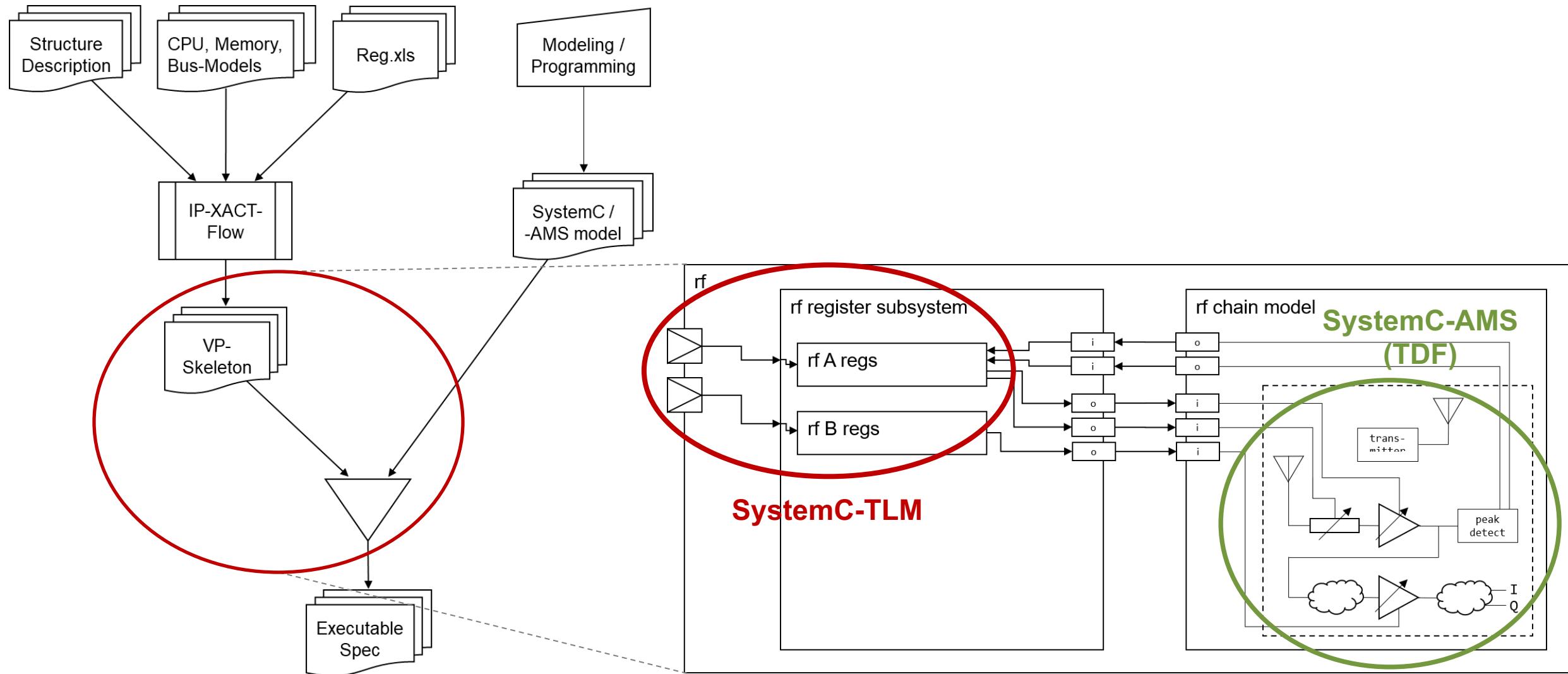
SYSTEM INTEGRATION



SYSTEM INTEGRATION



SYSTEM INTEGRATION



System Simulation and Results



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LIBRARIES AND TECHNOLOGIES USED

- SystemC 2.3.x Implementation from EDA Tool
- SystemC-AMS 2.4 Implementation from EDA Tool
- IP-XACT system integration flow (incl build- and register generation flow)
- EDA tooling for waveform analysis and debug
- In-house libraries developed for configuration, RF models and common utilities

SYSTEMC-AMS MODEL EXAMPLE

```
#include <systemc>
#include <systemc-ams>

template <class T>
class decimator_tdf : public sca_tdf::sca_module {

public:
    sca_tdf::sca_in<T> tdf_i;
    sca_tdf::sca_out<T> tdf_o;

    decimator_tdf(sc_core::sc_module_name, unsigned int fir_len,
                  const T *coeff_,
                  unsigned int dec_factor_,
                  unsigned int out_scale_);

    ~decimator_tdf();
    void processing();
    void initialize();
    void set_attributes();

private:
    T *mem;
    T *coeff;
    unsigned int fir_len;
    unsigned int dec_factor;
    unsigned int out_scale;
};
```

Decimator implementation in
SystemC-AMS TDF

```
#include "decimator.h"

#include <cassert>
#include <cstring>

template <class T>
decimator_tdf<T>::decimator_tdf(sc_core::sc_module_name,
                                  unsigned int filter_len_,
                                  const T *coeff_,
                                  unsigned int dec_factor_,
                                  unsigned int out_scale_)

: tdf_i("tdf_i"),
tdf_o("tdf_o"),
fir_len(filter_len_),
dec_factor(dec_factor_),
out_scale(out_scale_)

{
    assert(filter_len_ >= dec_factor_);
    mem = new T[fir_len];
    coeff = new T[fir_len];
    memset(mem, 0, sizeof(T)*fir_len);
    memcpy(coeff, coeff_, sizeof(T)*fir_len);
}

template <class T>
decimator_tdf<T>::~decimator_tdf() {
    delete[] mem;
    delete[] coeff;
}

template <class T>
void decimator_tdf<T>::processing() {
    memmove(&(mem[dec_factor]), &(mem[0]), sizeof(T)*(fir_len-1));

    unsigned int i;
    for ( i = 0; i < dec_factor; i++ ) {
        mem[dec_factor-(i+1)] = tdf_i.read(i);
    }

    T output = (T)0;
    for( i = 0; i < fir_len; i++ ) {
        output += coeff[i] * mem[i];
    }

    tdf_o.write(output/out_scale);
}

template <class T>
void decimator_tdf<T>::initialize() { }

template <class T>
void decimator_tdf<T>::set_attributes() {
    tdf_i.set_rate(dec_factor);
    tdf_o.set_rate(1);
}

template class decimator_tdf<double>;
```

AGC LOOP CONTROL FIRMWARE EXAMPLE

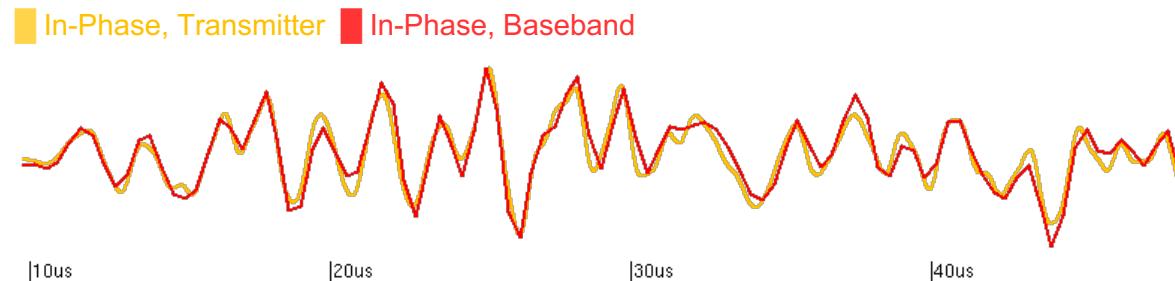
```
1 #include "timer.h"
2 #include "rf_A_regs.h"
3 #include "rf_B_regs.h"
4
5 rf_A_reg_t *rf_A_reg =
6     ((rf_A_reg_t *)RF_A_BASEADDRESS);
7
8 rf_B_reg_t *rf_B_reg =
9     ((rf_B_reg_t *)RF_B_BASEADDRESS);
10
11 const double gain_steps[17][2] = { { 0, 0 },
12                                     { 0, 1 },
13                                     { 0, 3 },
14                                     { 0, 7 },
15                                     { 0, 15 },
16                                     { 0, 31 },
17                                     { 0, 63 },
18                                     { 0, 127 },
19                                     { 0, 255 },
20                                     { 1, 255 },
21                                     { 3, 255 },
22                                     { 7, 255 },
23                                     { 15, 255 },
24                                     { 31, 255 },
25                                     { 63, 255 },
26                                     { 127, 255 },
27                                     { 255, 255 } };
28
29 void set_gain(int i) {
30     rf_A_reg->attenuator = gain_steps[i][0];
31     rf_A_reg->lna       = gain_steps[i][1];
32 }
33
34 int main(void) {
35
36     unsigned int gain_thres = 42;
37
38     int gain_step = 0;
39     unsigned int lo_level;
40     unsigned int hi_level;
41
42     for (;;) {
43         sleep(49,"us");
44
45         lo_level = rf_B_reg->lo_level;
46         hi_level = rf_B_reg->hi_level;
47
48         if (hi_level > lo_level + gain_thres) {
49             gain_step++;
50             if (gain_step > 16) gain_step = 16;
51         }
52
53         if (lo_level > hi_level + gain_thres) {
54             gain_step--;
55             if (gain_step < 0) gain_step = 0;
56         }
57
58         set_gain(gain_step);
59
60         rf_B_reg->reset = 1;
61         rf_B_reg->reset = 0;
62     }
63
64     return 0;
65 }
66 }
```

AGC LOOP CONTROL FIRMWARE EXAMPLE

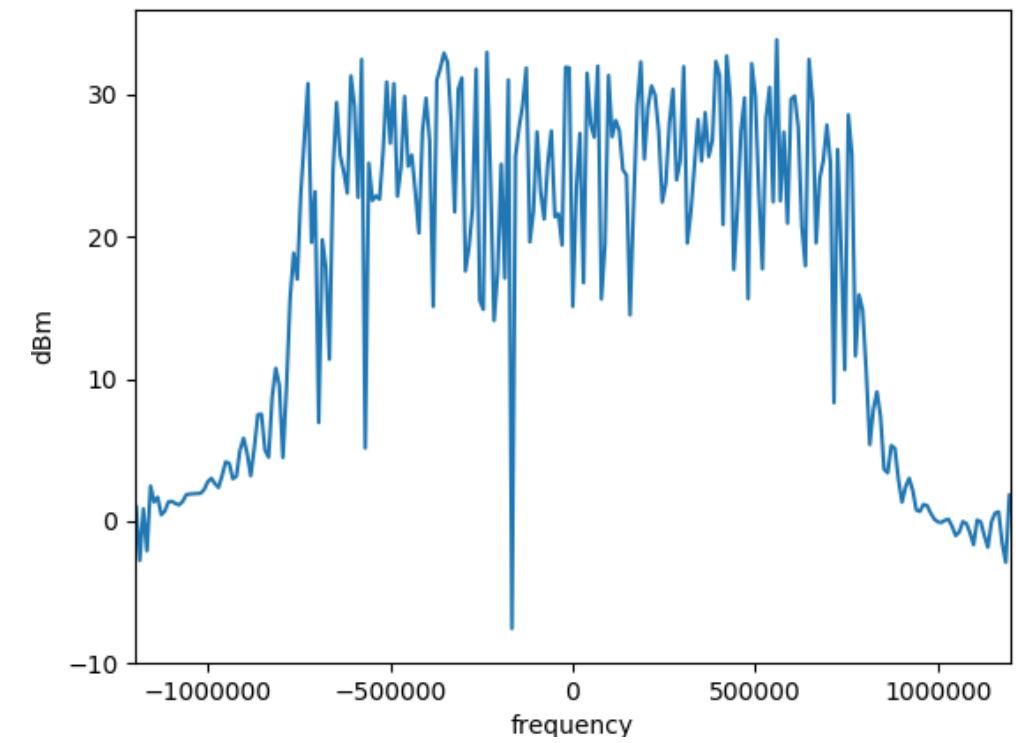
```
1 #include "timer.h"
2 #include "rf_A_regs.h"
3 #include "rf_B_regs.h"
4
5 lo_level = rf_B_reg->lo_level;
6 hi_level = rf_B_reg->hi_level;
7
8 if (hi_level > lo_level + gain_thres) {
9     gain_step++;
10    if (gain_step > 16) gain_step = 16;
11 }
12
13 if (lo_level > hi_level + gain_thres) {
14     gain_step--;
15    if (gain_step < 0) gain_step = 0;
16 }
17
18
19
20
21
22
23
24
25
26
27
28
29 void set_gain(int i) {
30     rf_A_reg->attenuator = gain_steps[i][0];
31     rf_A_reg->lna      = gain_steps[i][1];
32 }
33
34
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```

The diagram illustrates the flow of control between the main loop and the `set_gain` function. Red arrows originate from the `if` statements in the main loop and point to the corresponding sections within the `set_gain` function. Specifically, the first `if` statement in the main loop points to the first section of the `set_gain` function, and the second `if` statement points to the second section.

DAB TRANSMISSION SANITY CHECK: “UNITY GAIN” (NO AGC)



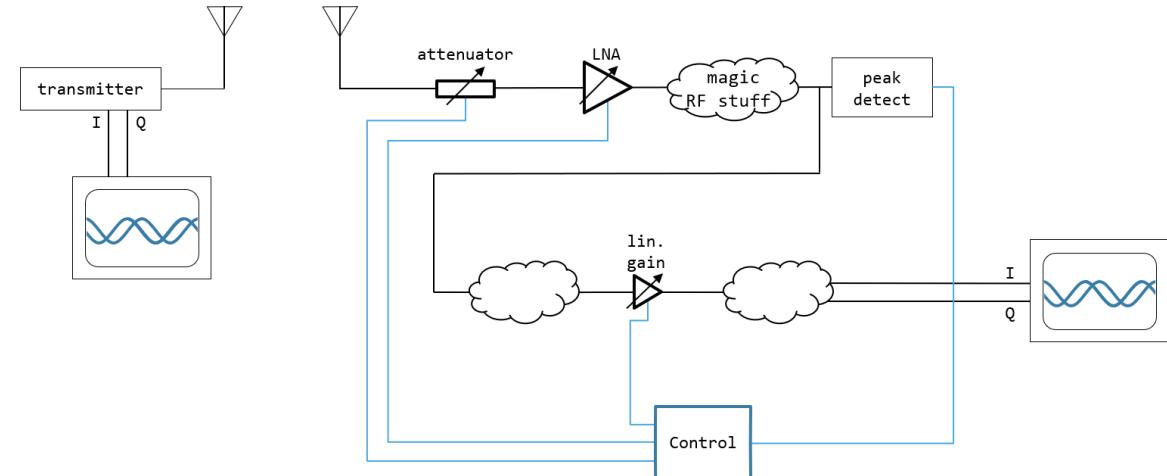
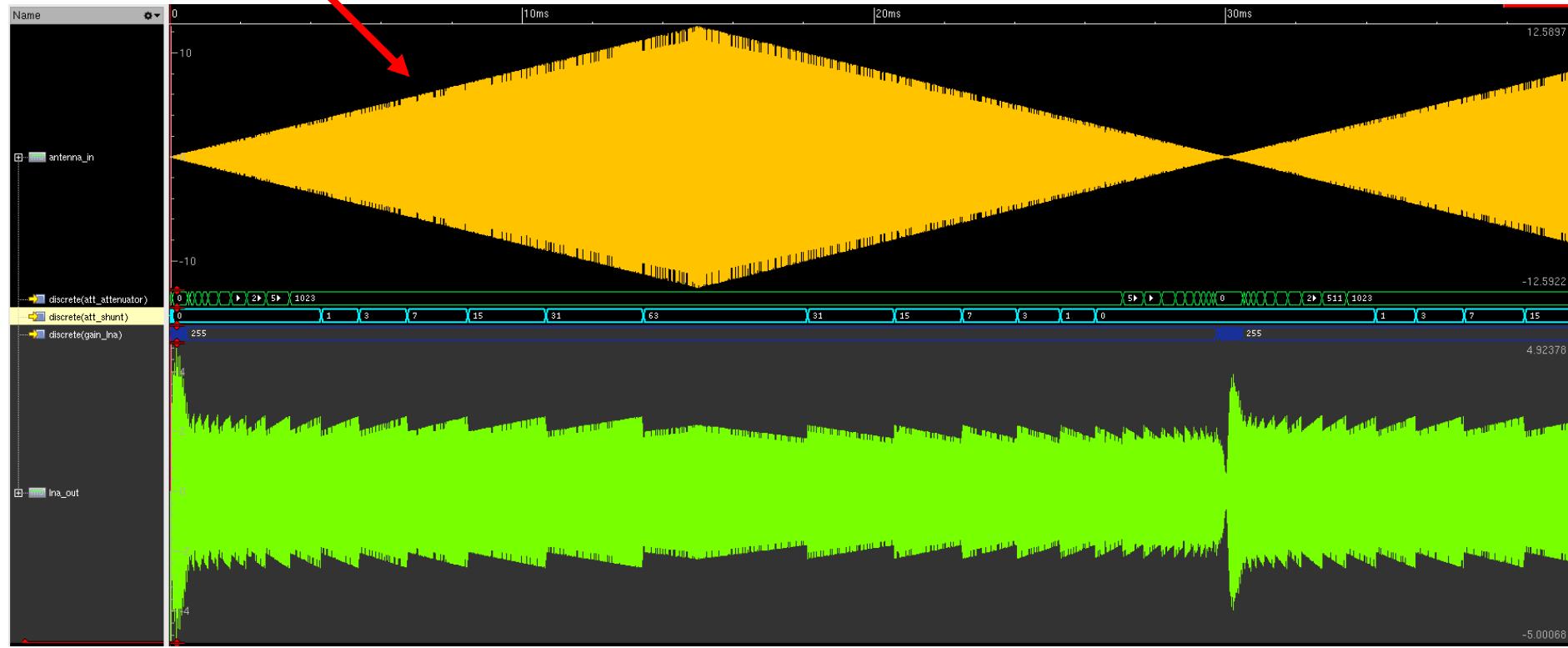
Time domain signal



Frequency domain signal

SYSTEM SANITY CHECK: AGC LOOP CONTROL

15 ms ramp
(full dynamic range)



RESULTS

- Modeled AGC loop in an RF-frontend
- System-level interaction: $\mu\text{C} \Leftrightarrow \text{RF-frontend}$
- PoC for early driver / FW development
- Simulation Speed:
 - Discrete Event-based: ~2 hrs processing for 1 sec radio stream
(passband signal representation)
 - TDF-based: ~10 min processing for 1 sec radio stream
(passband signal representation)



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