A COSIDE based (virtual) Radarsensor on the (virtual) Road

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2015-11-10; Munich; Coside UG Meeting

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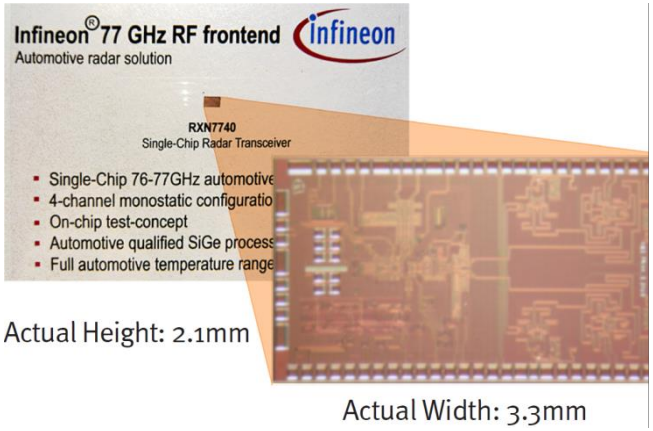
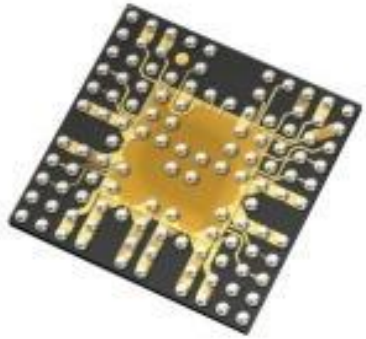
Purpose and Vision – Product 2 System

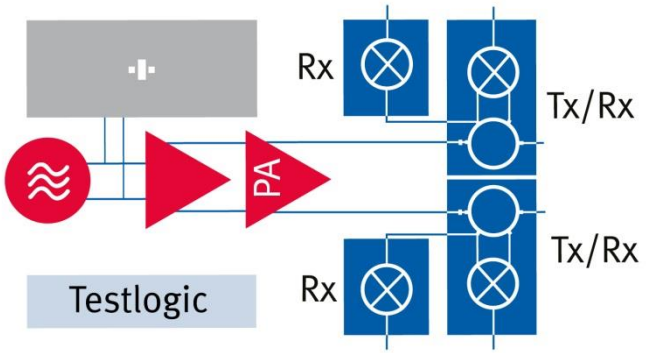
- Infineon's Radar Success Story:
- First IFX 77GHz Radar Sensor
  - 2003: 77GHz SiGe:C VCO
  - 2005: 77GHz Transmitter
    77GHz Receiver
  - 2006: **77GHz 2RX 2TRX + VCO Prototype**
  - 2009: series Product
    Porsche
    Panamera
  - 2012: SiGe:C + CMOS Companion
  - 2014: BiCMOS Integration



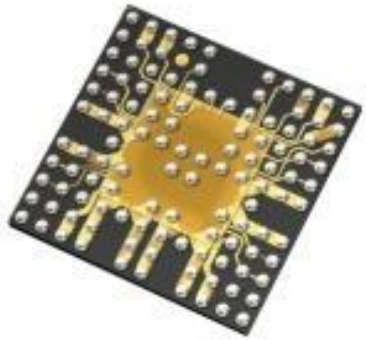


3rd Gen, Carrying the WORLD

- 3rd Gen. has done a great job!
- Support of 3rd Gen. RADAR
- Derivate solutions have supported 4th Gen. RADAR
- CMOS companion has enhanced functionality and flexibility to 3rd Gen. derivate solutions



- We think, it's time for 3rd Gen and its companion to retire
- The next generation shall contain all the knowledge in one design



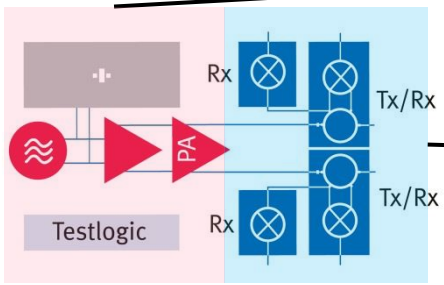
Historic Attempts?

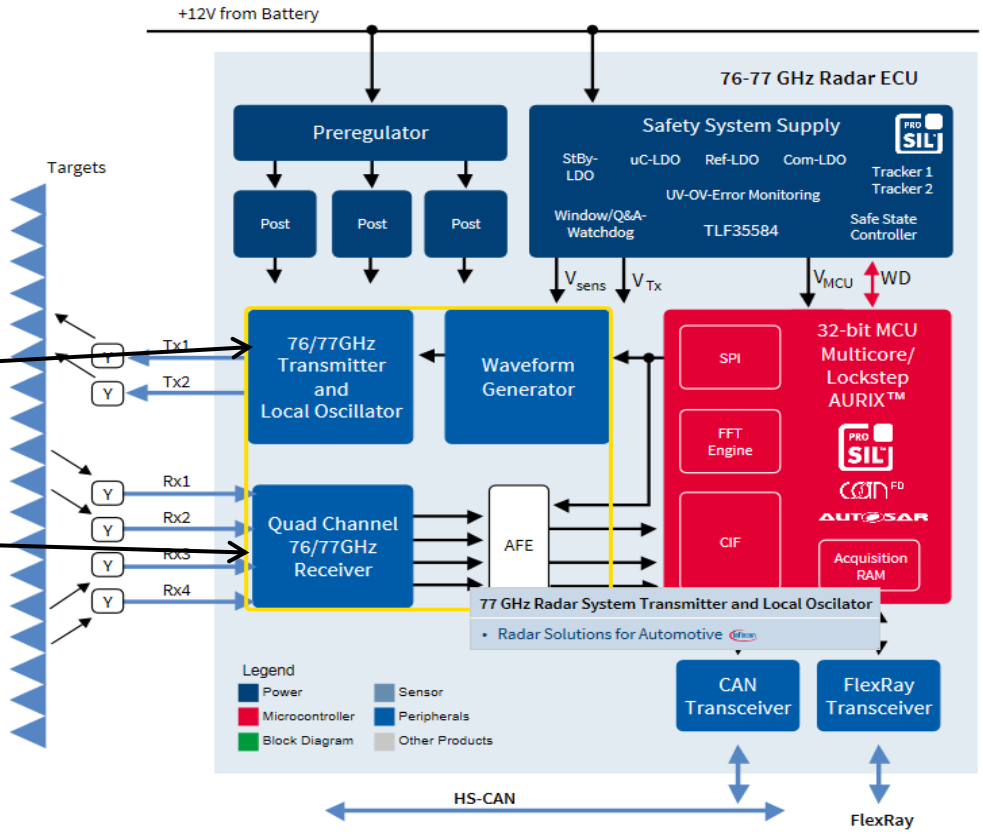
- Customer demands product with very brief description
  - Brief and hard to fulfill specification
- Block concept with simple ideal simulation (Matlab ®, Simulink)
  - Demands to circuit design
  - Layout back annotation

- Test circuit → functional verification
  - Refinements
- Product
  - Lessons learned: some spec. values over demanded!
- Future: Pre-Sim and relax demands!

Generation 4 System Approach

- Infineon RADAR Products:
- Waveform Generator
- RF-Transmitter
- RF-Receiver



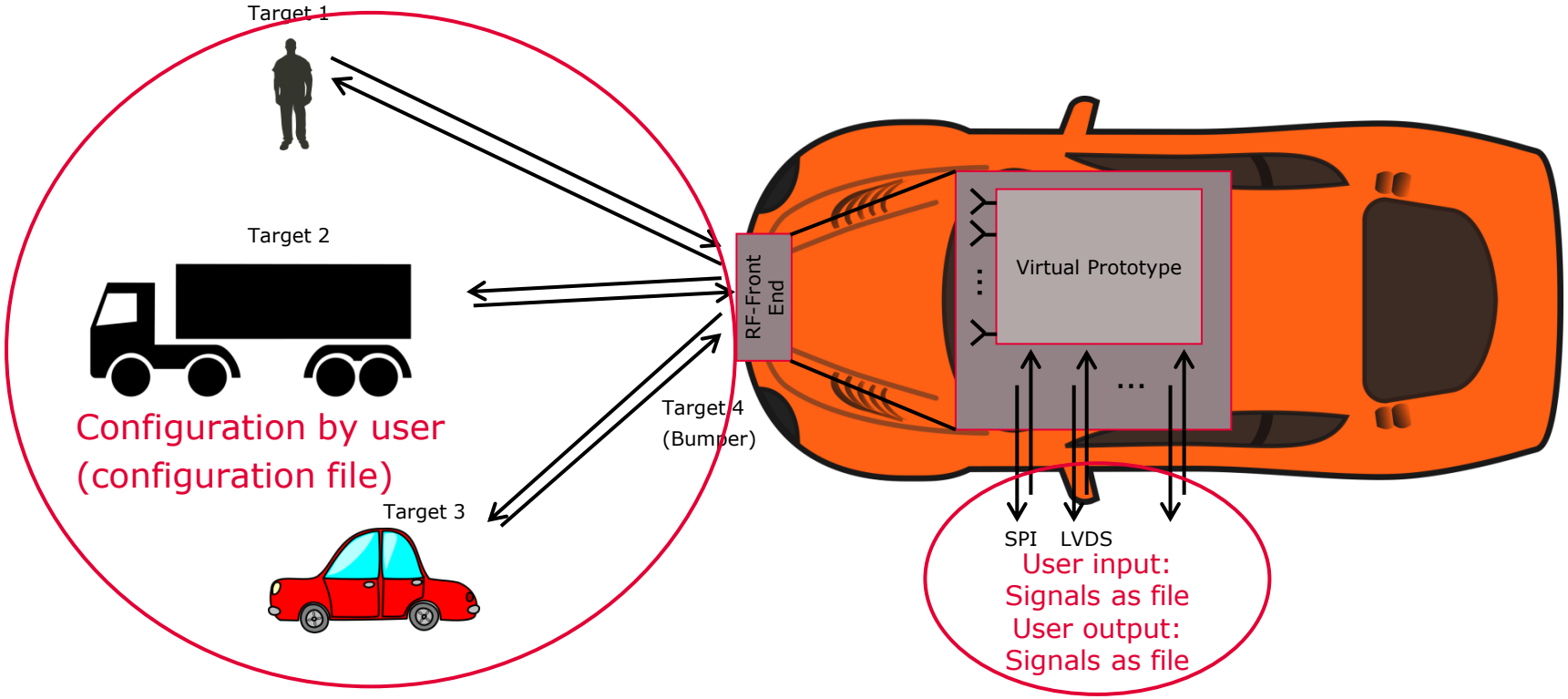


- No influence on
  - AFE+ADC+DFE
  - Microcontroller
  - Power supply
  - Com. Interface

- Gen. 5 to be supported

What is the Virtual Prototype?

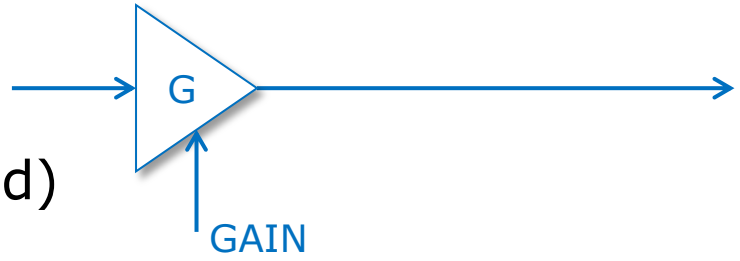
- **The Virtual Prototype is a computer simulation model (software) that is a complete bit- and cycle-accurate, functional model of the RADAR chip and includes a simple channel model (target scenario).**

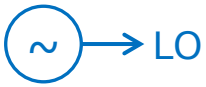


- Same interface as silicon chip on PIN level
- Same programming as final hardware (via SPI)

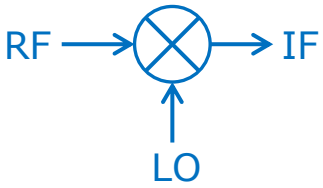
VP – Design Insights (1/3)

- How is the virtual prototype designed?
- blocks are known (Core Concept defined)
  - basic functionality is known too
  - models are implemented from simple to sophisticated
  - level 1: basic function – examples

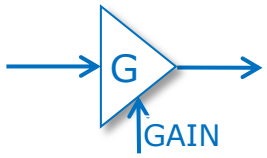




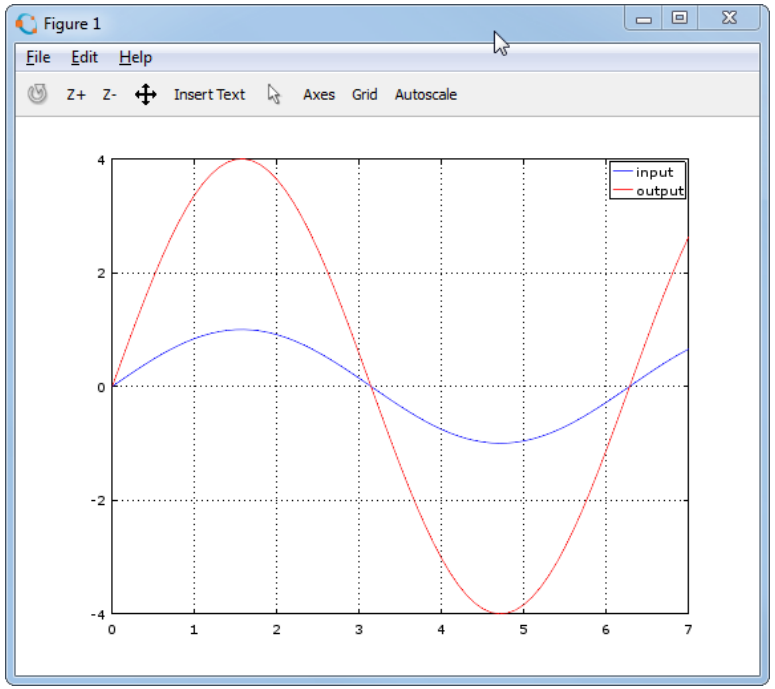
$$s_{\mathrm{LO}} = \hat{V}\,\sin\left(2\,\pi\,f_{\mathrm{LO}} + \phi\right)$$



$$s_{\mathrm{IF}} = s_{\mathrm{LO}} \cdot s_{\mathrm{RF}} \cdot G_{\mathrm{lin}}$$

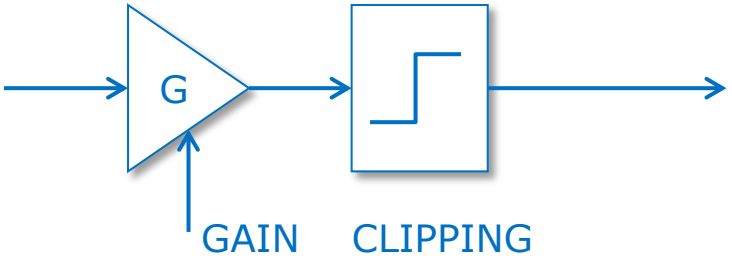


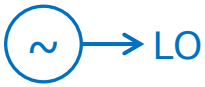
$$s_{\mathrm{out}} = s_{\mathrm{in}} \cdot G_{\mathrm{lin}}$$



VP – Design Insights (2/3)

- saturation modelled using polynomal fitting methods.
  - model calculated @ VP init
  - model 2 be interchanged with design update
  - level 2: non-linearities are partly taken into account

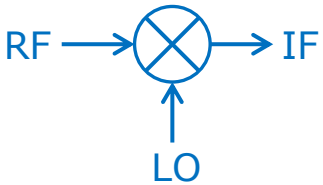




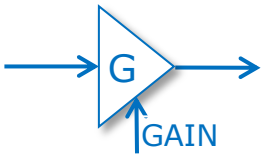
$$\varphi \sim \mathcal{N}(0, \sigma_\varphi^2)$$

$$s_{\mathrm{LO}} = \hat{V} \sin\left(2\pi f_{\mathrm{LO}} + \phi + \varphi\right)$$

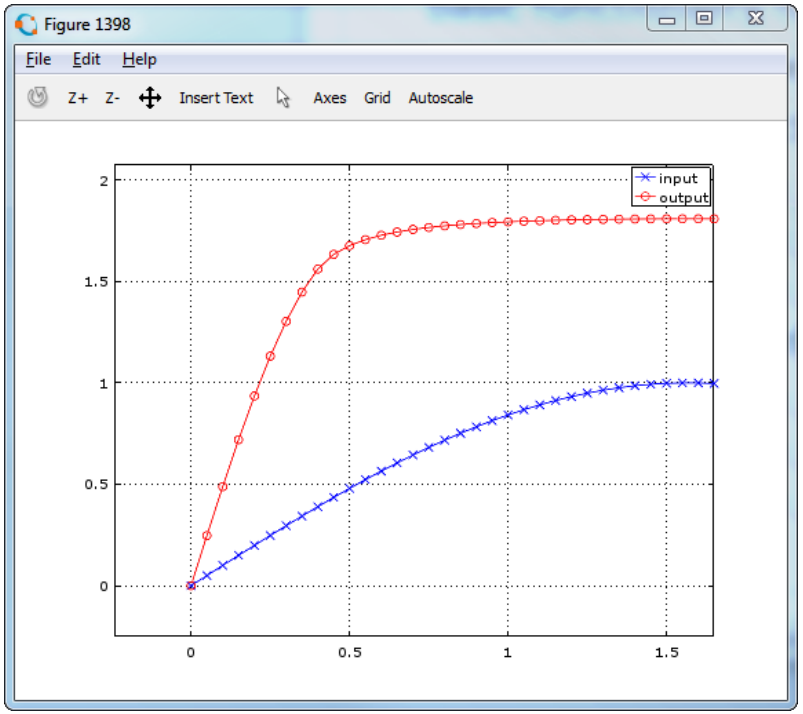
$$= \hat{V} \sin\left(2\pi f_{\mathrm{LO}} + \phi\right) + \omega_{\mathrm{AWGN}}$$



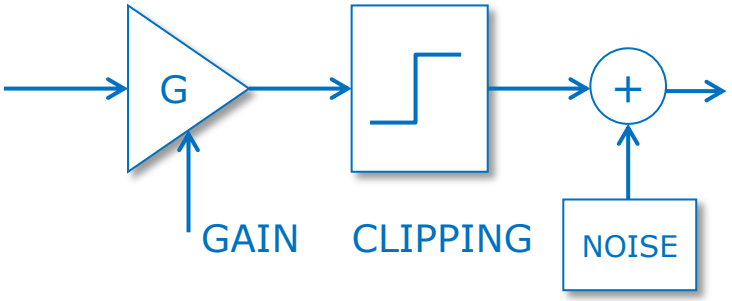
$$s_{\mathrm{IF}} = s_{\mathrm{LO,sat}} \cdot s_{\mathrm{RF,sat}} \cdot G_{\mathrm{lin}}$$



$$s_{\mathrm{out,sat}} = \sum_{i=0}^{P} a_i \cdot s_{\mathrm{in}}^i \cdot G_{\mathrm{lin}}$$



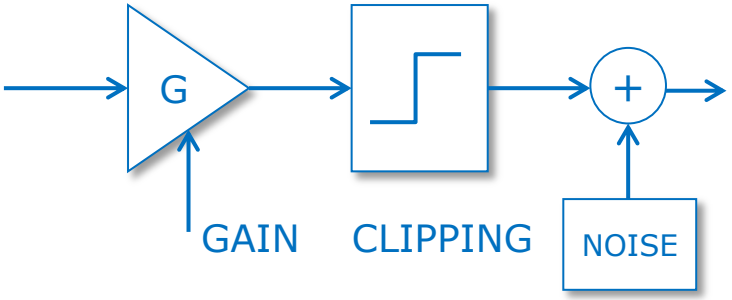
VP – Design Insights (3/3)



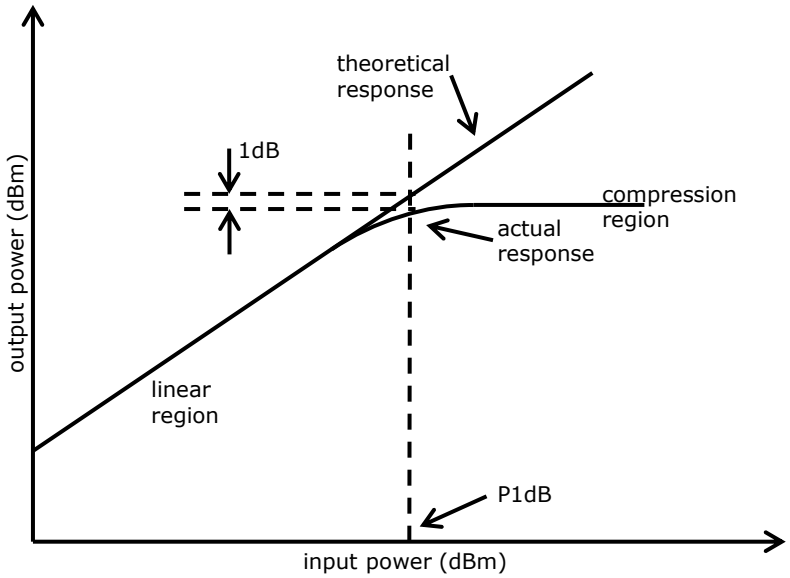
- implementation levels 3 & 4
  - level 3: higher order non-linearities are modelled as add-on to the clipping behavior
  - level 4: noise is taken into account (defined via Noise Figure)

- Computational Effort: e.g. amplifier
  - level 1: 1 mult.
  - level 2: 1 mult. + if then else statement
  - level 3: 3 mult. + 2 adds + if then else statement
    - can be even more complicated, depends on composition of model
  - level 4: 4 mult. + 3 adds + if then else statement

VP – Design Insights - Conclusion

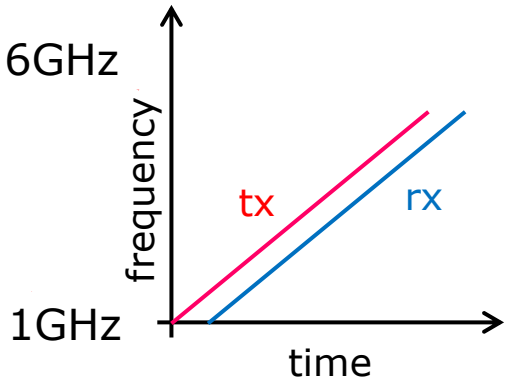


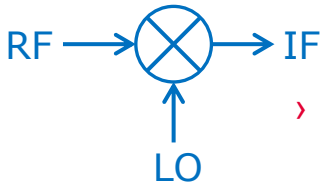
- Several implementations possible:
  - level 1: simple amplification variable on simulation start
  - level 2: …add clipping shift-able
  - level 3: … simulation data to be used on start & interchangeable with csv files from designers
    - polynomial fitting algorithms used to fetch P1dB behavior from design files or measurement results
  - level 4: serval random gen. solutions are available to vary possible close to reality behavior



Simulation Insights

- improving speed @ same quality of data?
- relax carrier frequency demands



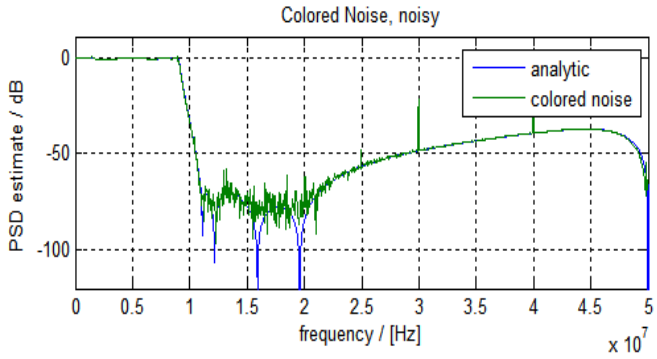


- CONDITION: same ramp steepness & bandwidth!

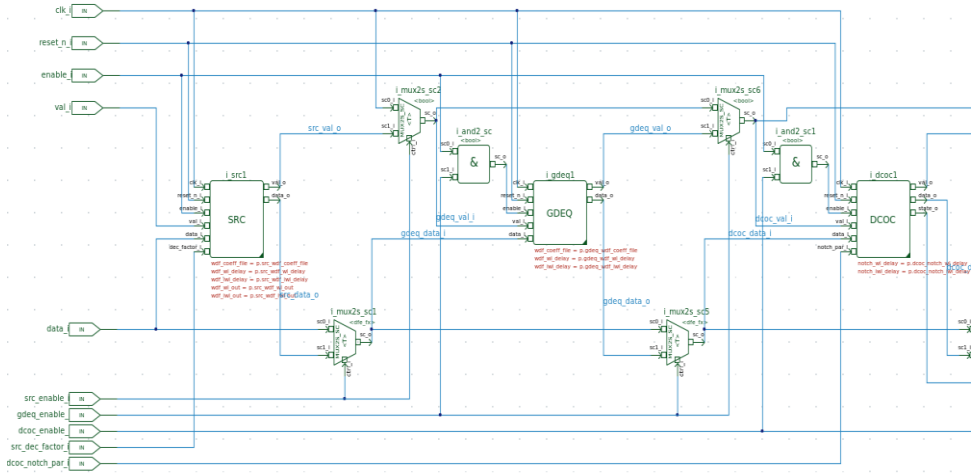
  - shift virtual LO to lower value ➔ run simulation
    - same number of samples for "lower" frequency @ more time between two steps
    - digital core computation is calced at virtual real time
  - backscale result to value as if has been simulated at actual LO

Problem Formulation

- Our digital design consists of three stages:
  - Concept



  - Virtual Prototype (Coside / SystemC)
  - Realization (design) in VHDL or others

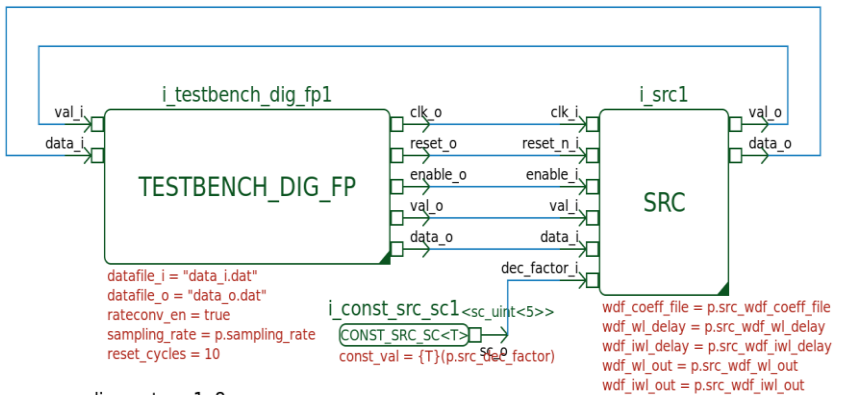


- We need to make sure, each of them works, according to
  - the draft
  - customer requirements

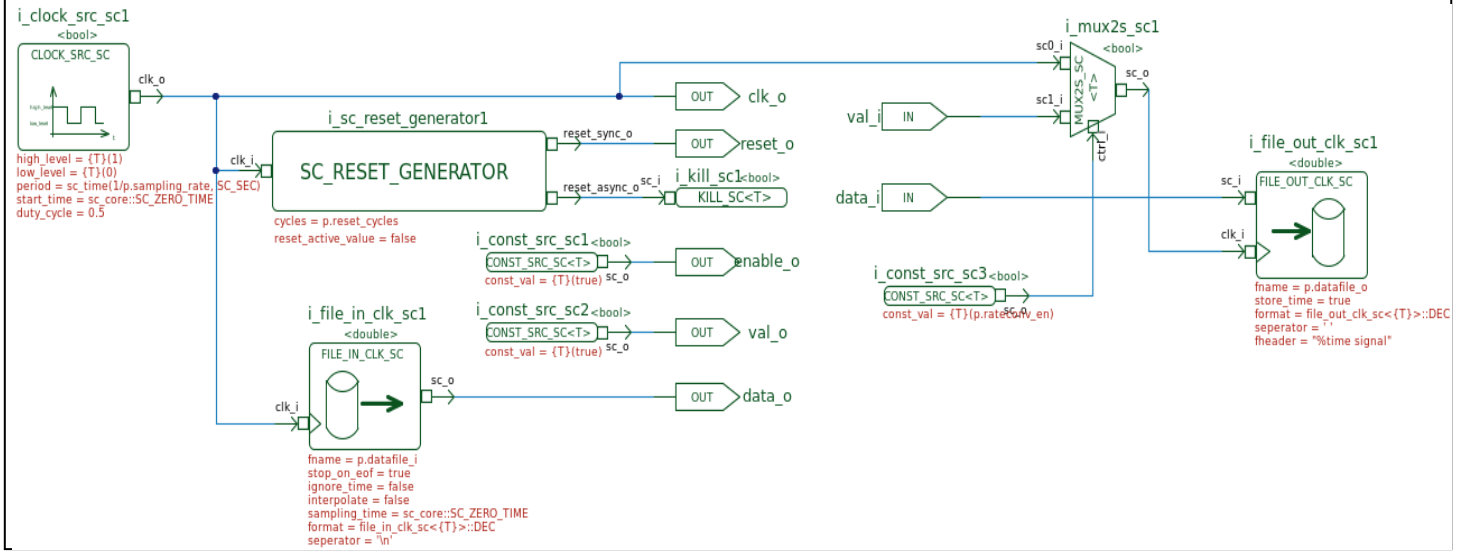
Verification with Virtual Prototype (I)

- Module under test is connected to the test bench module, which handles input to and output from the module with data files
- Available test bench modules:
  - *test_bench_dig*
  - *testbench_dig_fp*
    test bench for fixed point modules
  - *testbench_dig_hiprec*
    file out with high decimal precision

test bench connected to the SRC module



schematic of test_bench_dig

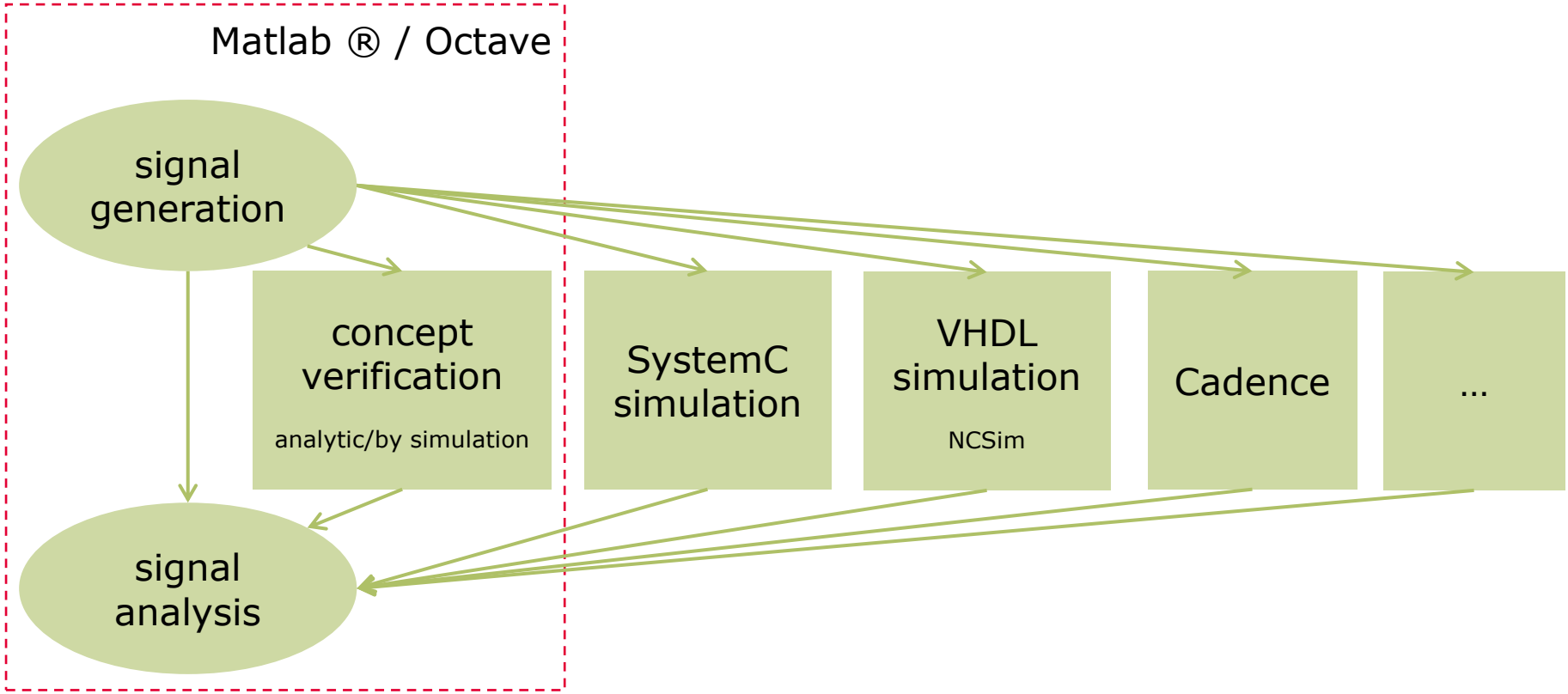


Design Verification

- Power Up sequence applied to both, CV and circuit simulation
  - Comparison of signals highlights divergence from concept
  - Timing issues can be tracked easily
- Virtual world scenarios mirror behavior of real world scenarios and help to find measurement and test cases
- Digital domain regression be formulated
  - CRC verification
  - CRC test-cases be defined for measurement
- ROM code of FW to be applied to VP
  - Test routines be evaluated before first silicon arrives

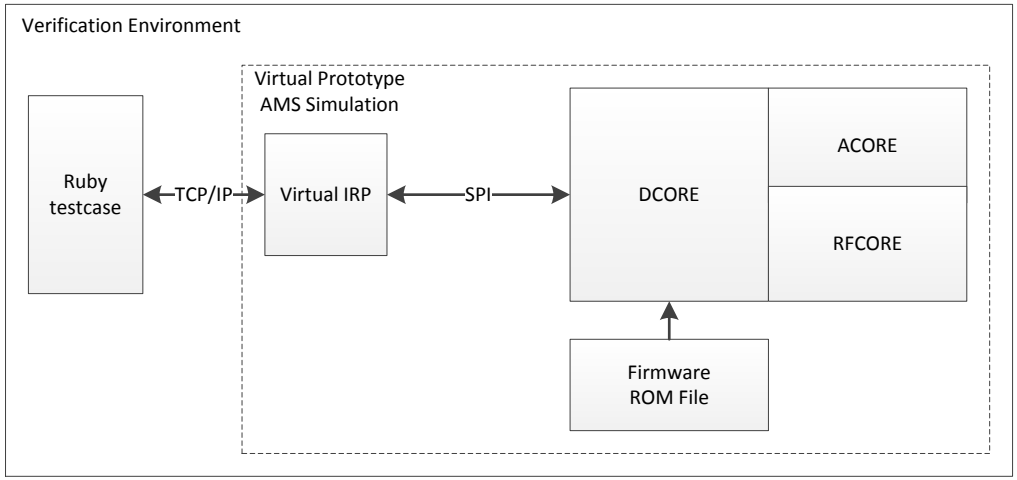
Concept and Design Verification

› Matlab ® based verification framework



Firmware functions developed on VP

- VP used to verify FW functionality
- Virtual IRP already verified
- Test cases used to cross-verify circuit wiring and consistency of concept with design
- Firmware development starts with completion of basic VP version and is preceded and refined with each enhancement of the VP
- Less updates ➔ gains time & money



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