



A virtual prototyping methodology for timing-accurate simulation of AMS circuits

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07/12/23



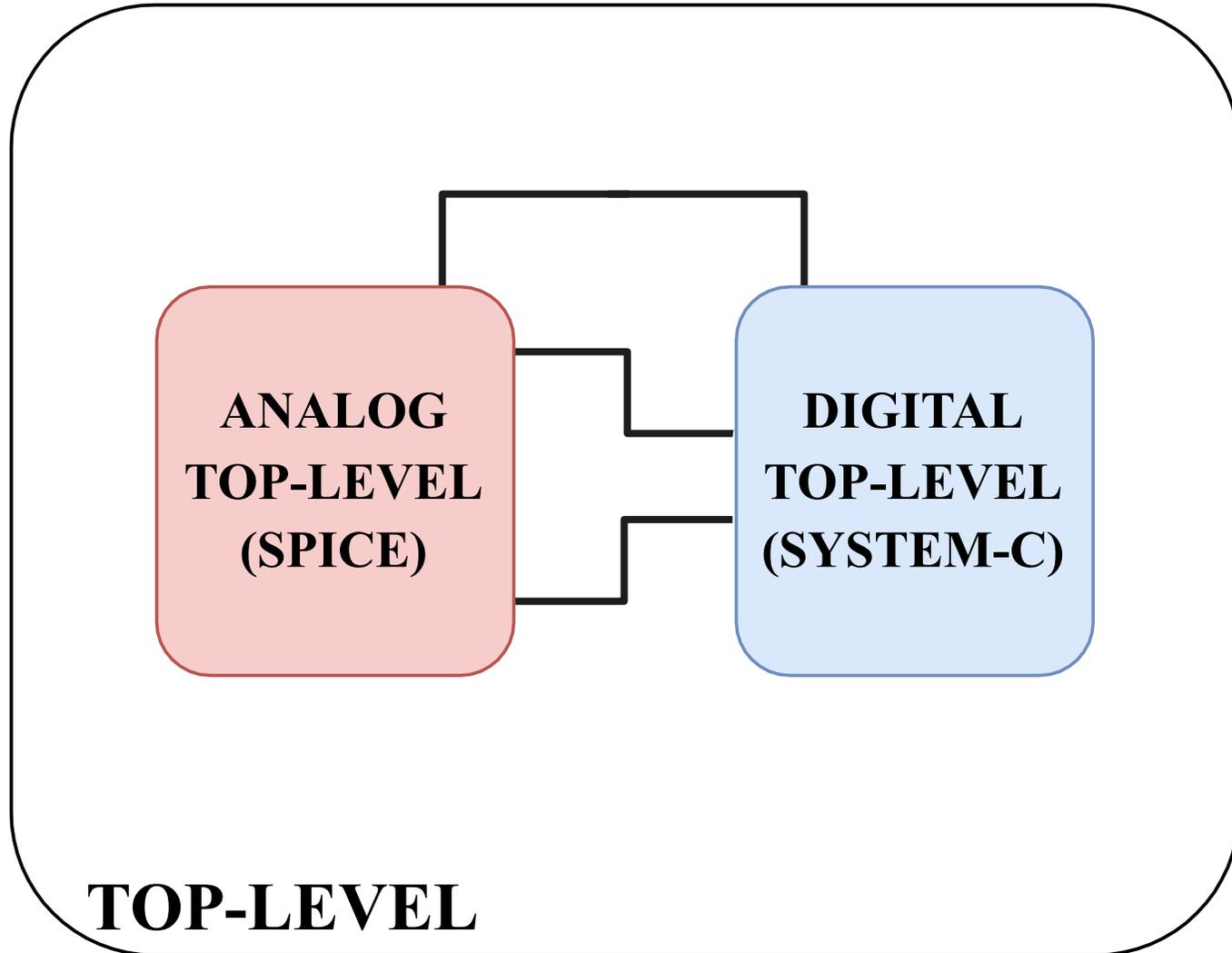
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Solution: Abstraction of Digital Circuits



- Adds timing checks to digital elements (i.e., flip-flops)
- Maintains digital circuits' timing accuracy (Liberty Data)
- Maintains analog circuits' overall accuracy (kept in SPICE)
- Increases simulation speed (Discrete Events-based digital simulator)
- Improves reusability (library of sub-circuits)

Requirements: Inputs

Liberty Database

```

1 | cell ("sky130_fd_sc_hs__and2_1") {
2 |   area : 7.992;
3 |   ...
4 |   pin ("A") {
5 |     direction : "input";
6 |     capacitance : 0.0024;
7 |     internal_power () {...} ...
8 |   }
9 |   pin ("X") {
10|     direction : "output";
11|     function : "(A&B)";
12|     ...
13|     timing () {
14|       cell_fall ("delay_template13x20") {
15|         index_1("0.01, 0.01735, ...");
16|         index_2("0.00, 0.00841, ...");
17|         values("0.05541, 0.0872, ...",
18|             "0.05756, 0.08938, ...", ...
19|       } ... } ... } ... }

```

SPICE-level Netlist

```

1 | .include "sky130_fd_pr__nfet_01v8_lvt__tt.spice"
2 | ...
3 | .SUBCKT sky130_fd_sc_hs__and2 A B X VGND VNB VPB VPWR
4 |   MMP0 y A VPWR VPB pfet_01v8 m=1 w=0.84 l=0.15 ...
5 |   MMP1 y B VPWR VPB pfet_01v8 m=1 w=0.84 l=0.15 ...
6 |   MMN0 y A sndA VNB nfet_01v8_lvt m=1 w=0.64 l=0.15 ...
7 |   MMN1 sndA B VGND VNB nfet_01v8_lvt m=1 w=0.64 l=0.15 ...
8 |   MMIP0 X y VPWR VPB pfet_01v8 m=1 w=1.12 l=0.15 ...
9 |   MMIN0 X y VGND VNB nfet_01v8_lvt m=1 w=0.74 l=0.15 ...
10| .ENDS sky130_fd_sc_hs__and2_1
11| ...
12| .SUBCKT TopLevel6288 A0 A1 ... P31 VGND VNB VPB VPWR
13|   X0 A3 B0 net1 VGND VNB VPB VPWR sky130_fd_sc_hs_nand2
14|   ...
15|   X6 A1 B4 net27 VGND VNB VPB VPWR sky130_fd_sc_hs_and2
16|   ...
17|   X84 B12 A0 P6 VGND VNB VPB VPWR sky130_fd_sc_hs_xnor2
18| .ENDS TopLevel6288

```

SystemC-AMS & COSIDE Environment

- Design, compile, simulate and verify SystemC(AMS) code
- Drag and drop blocks in a schematic
- Create behavioral models for mixed-signal circuits
- Integration with SPICE, other HDLs...
- HW/SW co-simulation, ability to model electrical and mechanical parameters...

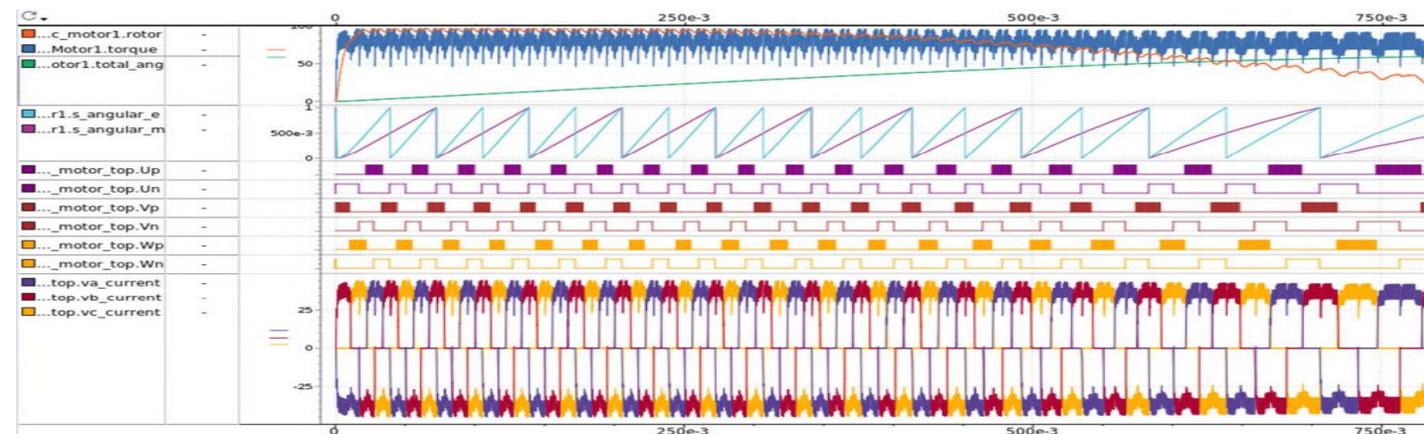
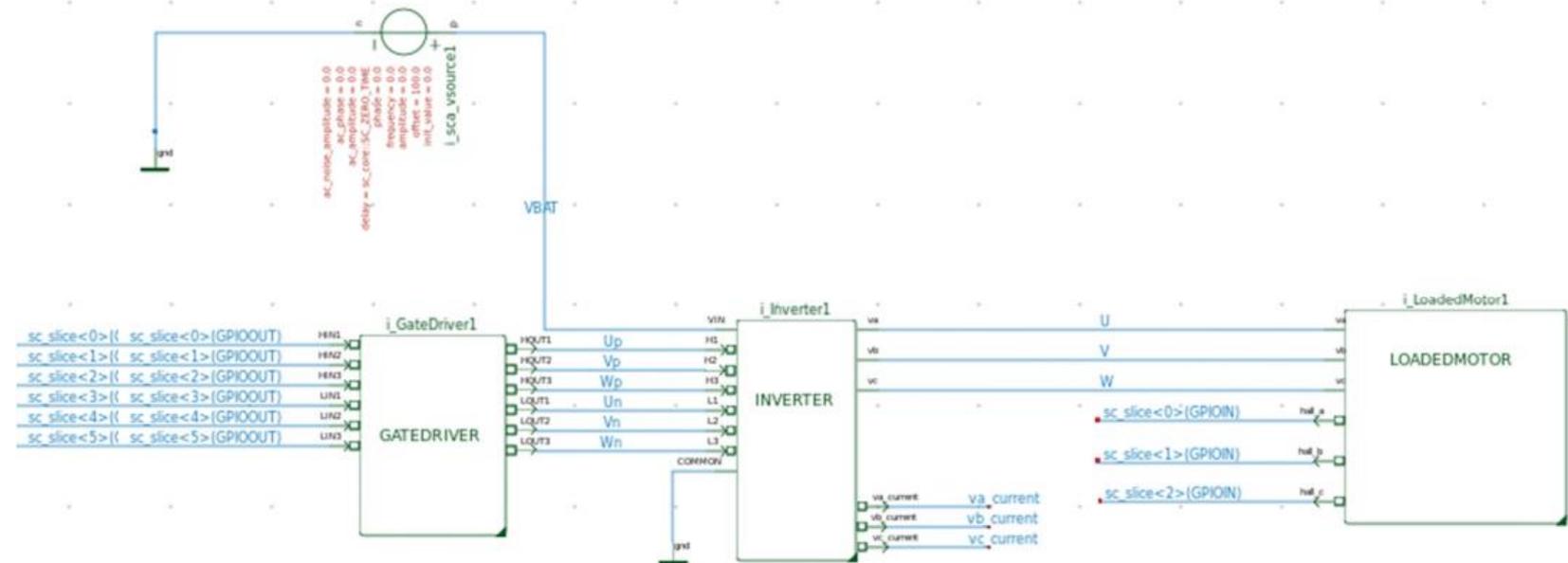
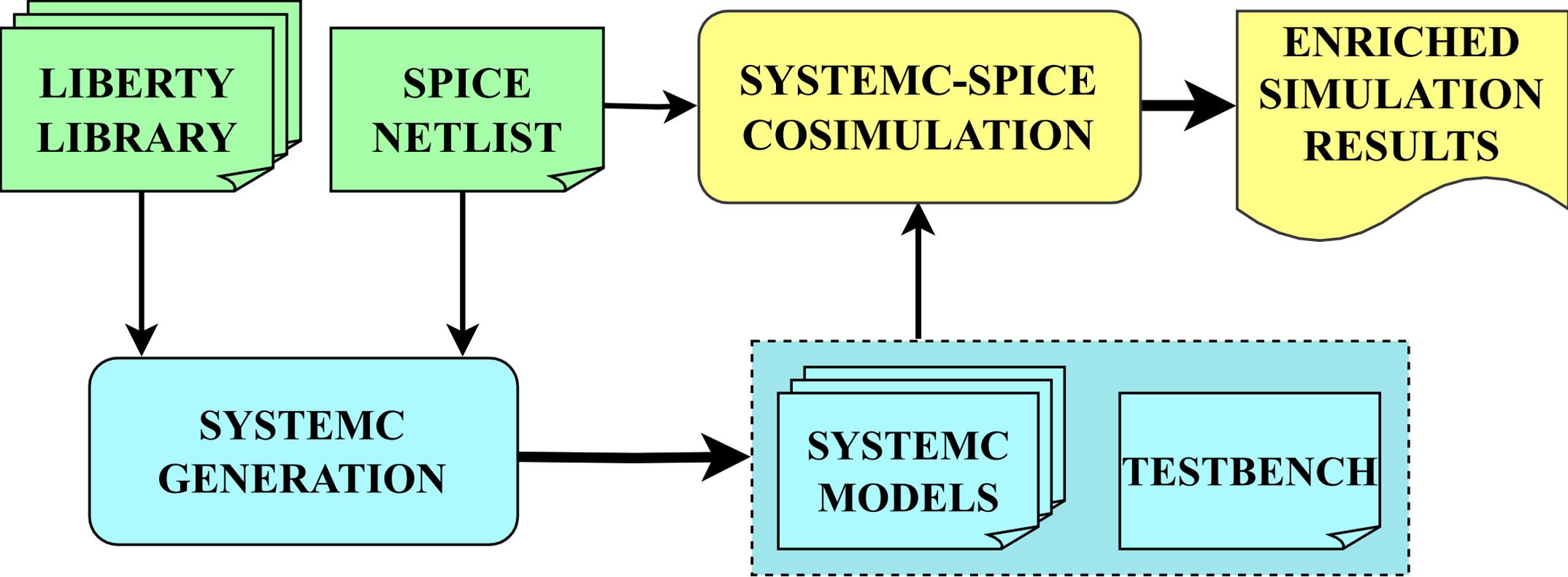


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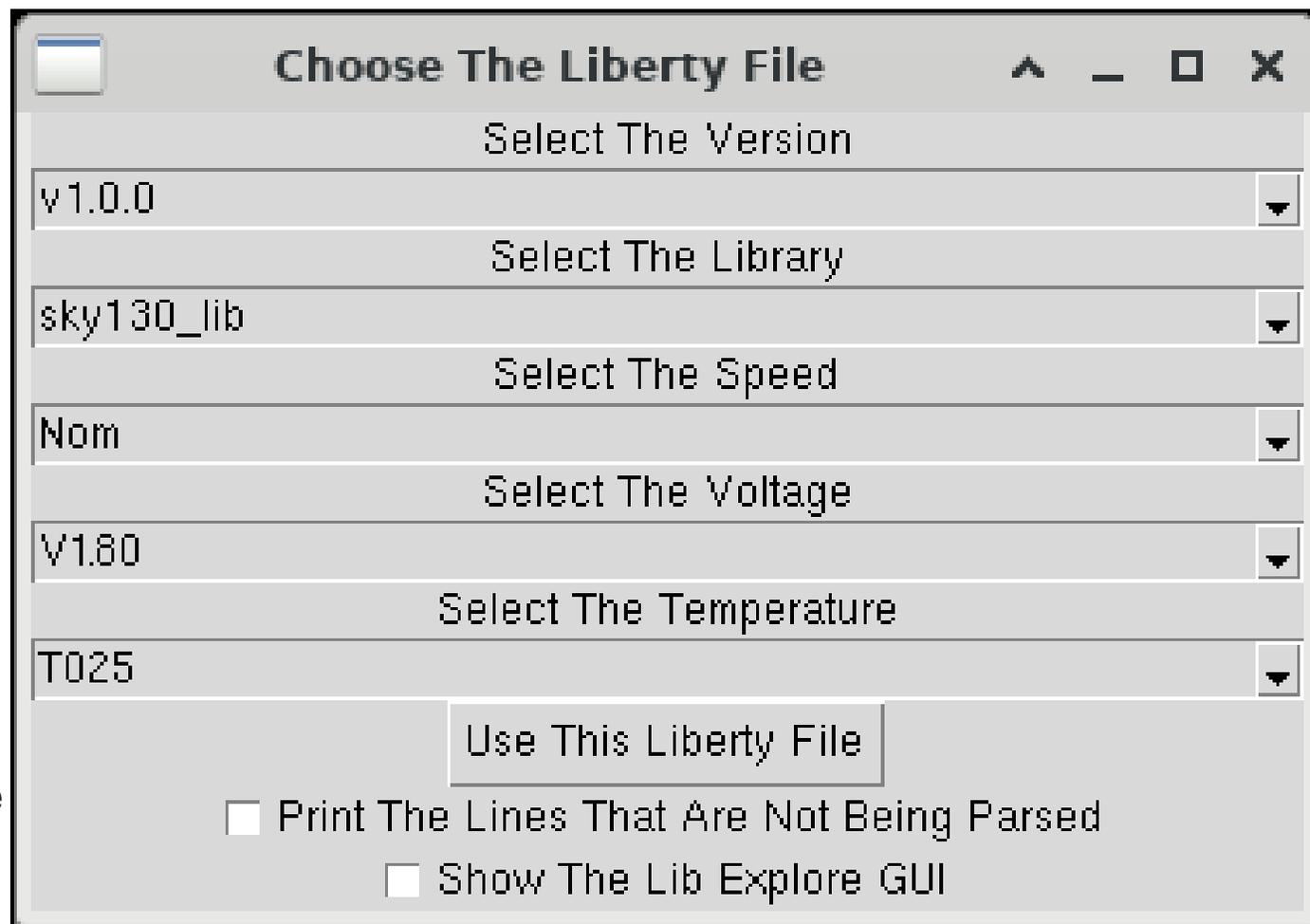
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Proposed methodology (0): Top-level View



Proposed methodology (1): Select PVT Corner

- Cell libraries are typically described with multiple corners
- Characterization at different Voltages, Temperatures and with different Process quality
- Many corners to predict the behavior of the system in both nominal conditions and in the most extreme ones
- The library of SystemC standard cells will use a single, selectable corner



Proposed methodology (2): Parse Liberty

Cells, Pins & Parameters	Path To Reach This Element
sky130_fd_sc_hs_a41oi_1	cell_list[67].name
sky130_fd_sc_hs_a41oi_2	cell_list[68].name
sky130_fd_sc_hs_a41oi_4	cell_list[69].name
sky130_fd_sc_hs_and2_1	cell_list[70].name
Area=7.9920000000	cell_list[70].area
Avg_Leak_Power=0.1384900000	cell_list[70].pleak_avg
Leak_Power_List	cell_list[70].pleak_values
Pin_List	cell_list[70].pin_list
A	cell_list[70].pin_list[0].name
B	cell_list[70].pin_list[1].name
X	cell_list[70].pin_list[2].name
OUTPUT	cell_list[70].pin_list[2].direction
Cap=0.0023000000	cell_list[70].pin_list[2].cap
Min_Cap=	cell_list[70].pin_list[2].min_cap
Max_Cap=0.1485900000	cell_list[70].pin_list[2].max_cap
Function:(A&B)	cell_list[70].pin_list[2].function
Timing_Features_List	cell_list[70].pin_list[2].timing_list
A	cell_list[70].pin_list[2].timing_list[0].name
Timing_Sense:positive_unate	cell_list[70].pin_list[2].timing_list[0].timing_sense
Cell_Fall	cell_list[70].pin_list[2].timing_list[0].idx2_list[0]
Fall_Transition	cell_list[70].pin_list[2].timing_list[0].idx2_list[1]
Cell_Rise	cell_list[70].pin_list[2].timing_list[0].idx2_list[2]
Rise_Transition	cell_list[70].pin_list[2].timing_list[0].idx2_list[3]
Output_Current_Fall	cell_list[70].pin_list[2].timing_list[0].I_fall_list
Output_Current_Rise	cell_list[70].pin_list[2].timing_list[0].I_rise_list
B	cell_list[70].pin_list[2].timing_list[1].name
Internal_Power_List	cell_list[70].pin_list[2].internal_power
sky130_fd_sc_hs_and2_2	cell_list[71].name

Time Unit: 1ns
Voltage Unit: 1V
Power Unit: 1nW
Current Unit: 1mA
Capacitance Unit: 1.000"pf"

List of library cells
(Dark Green)

Hierarchical
content of a cell
(Green -> Blue
Gradient)

Proposed methodology (2): Parse Liberty

Popup GUI for data in 1D vectors and 2D matrixes

Cells, Pins & Parameters	Path To Reach This Element
sky130_fd_sc_hs_a41oi_1	cell_list[67].name
sky130_fd_sc_hs_a41oi_2	cell_list[68].name
sky130_fd_sc_hs_a41oi_4	cell_list[69].name
sky130_fd_sc_hs_and2_1	cell_list[70].name
Area=7.9920000000	cell_list[70].area
Avg_Leak_Power=0.1384900000	cell_list[70].pleak_avg
Leak_Power_List	cell_list[70].pleak_values
Pin_List	cell_list[70].pin_list
A	cell_list[70].pin_list[0].name

List of library cells (Dark Green)

sky130_fd_sc_hs_and2_1 -> Pin_List -> X -> Timing_Features_List -> A -> Cell_Fall

```

Index_2("total_output_net_capacitance"): 0.0000000000 0.0084100000 0.0100900000 0.0121100000 0.0145300000 0.0174300000 0.0209100000
Index_1("input_net_transition"):
0.0100000000 0.0554100000 0.0872000000 0.0921600000 0.0979200000 0.1046300000 0.1125000000 0.1218000000
0.0173500000 0.0575600000 0.0893800000 0.0943200000 0.1000700000 0.1067800000 0.1146300000 0.1239300000
0.0260200000 0.0603800000 0.0921500000 0.0970900000 0.1028600000 0.1095800000 0.1174500000 0.1267300000
0.0390300000 0.0649600000 0.0967000000 0.1016400000 0.1074100000 0.1141400000 0.1220100000 0.1313100000
0.0585500000 0.0722000000 0.1039100000 0.1088700000 0.1146500000 0.1213700000 0.1292600000 0.1385800000
0.0878200000 0.0829800000 0.1148200000 0.1198200000 0.1256000000 0.1323300000 0.1402600000 0.1495900000
0.1317200000 0.0964900000 0.1298200000 0.1348700000 0.1407000000 0.1474900000 0.1554400000 0.1647900000
0.1975700000 0.1125400000 0.1481500000 0.1534100000 0.1594800000 0.1664900000 0.1746200000 0.1841000000
0.2963400000 0.1318100000 0.1703100000 0.1757900000 0.1820700000 0.1892900000 0.1976200000 0.2073200000
0.4444900000 0.1556800000 0.1976400000 0.2034400000 0.2100300000 0.2175300000 0.2261200000 0.2360500000
0.6667000000 0.1864100000 0.2321600000 0.2384200000 0.2454300000 0.2533300000 0.2623000000 0.2725600000
1.0000000000 0.2270700000 0.2769700000 0.2837700000 0.2913700000 0.2998700000 0.3093700000 0.3200700000
1.5000000000 0.2819000000 0.3365000000 0.3440000000 0.3523000000 0.3616000000 0.3719000000 0.3833000000

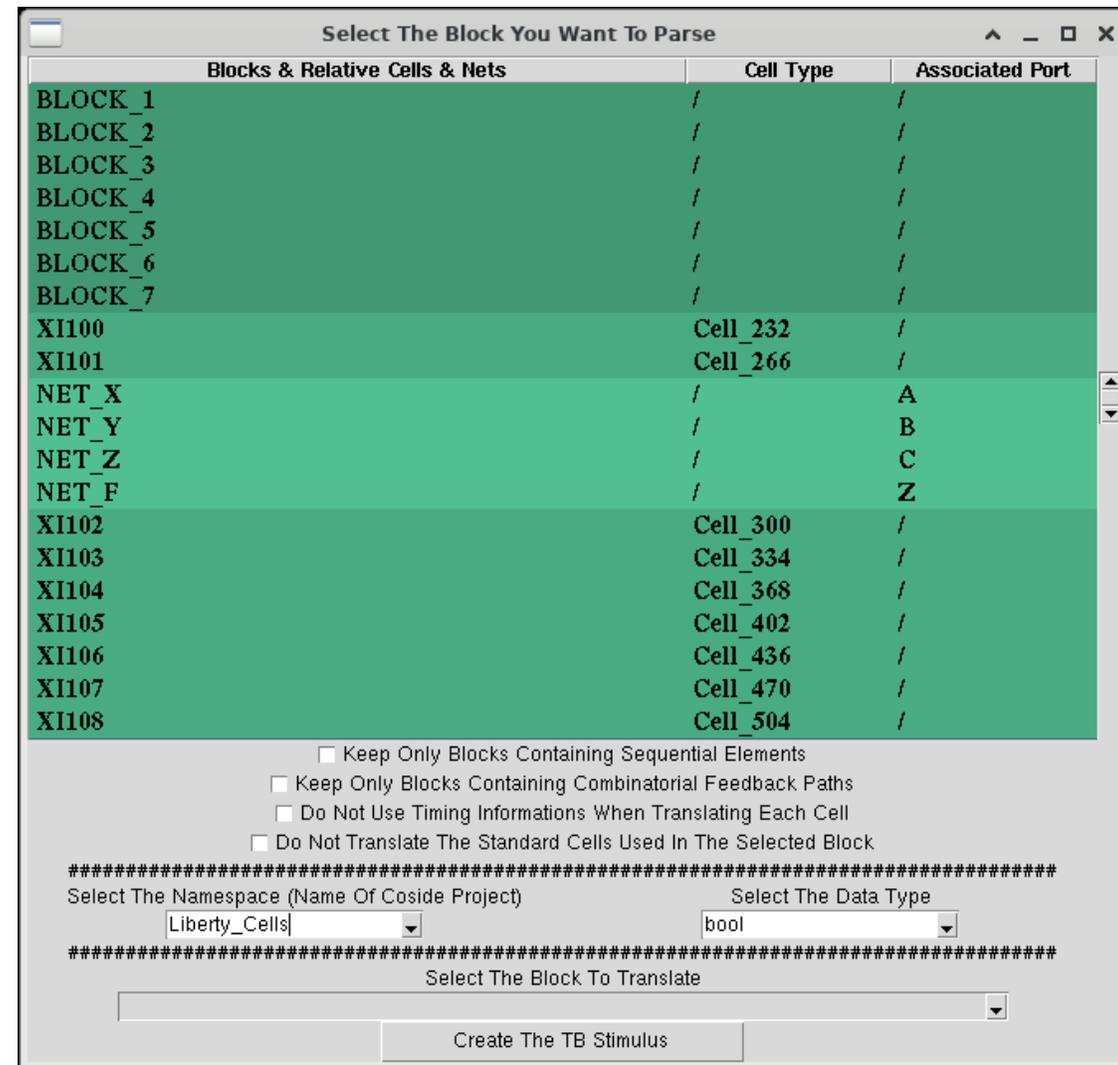
```

hierarchical content of a cell (Green -> Blue Gradient)

sky130_fd_sc_hs_and2_2	cell_list[71].name
Time Unit: 1ns	
Voltage Unit: 1V	
Power Unit: 1nW	
Current Unit: 1mA	
Capacitance Unit: 1.000"pf"	

Proposed methodology (3): Parse Netlist

- The script searches for blocks made of standard cells, filtering out the rest
- From each block we sample data about its cells' connections (wires, types of cells, names...)
- Synergy with Liberty data to distinguish INs from OUTs at both cell-level and block-level
- One block is selected and translated to SystemC using the same topology as the netlist



Proposed methodology (4): Testbench Generator

Create The Testbench Stimulus

Inputs	Initial Conditions (Reference: Start Of Sim)	Clock Specs & Number Of Intervals (Time Reference: Start Of Sim)																
Port_0	Starts At Logic Level '0' <input type="text" value="0"/>	Time Before 1st Edge [NS] <input type="text" value="3189.8"/> Semiperiod At '1' [NS] <input type="text" value="45.988"/>																
<input type="text" value="Clock"/>	Goes From 'X' To '0' After: [NS] <input type="text" value="0"/>	Number Of Full Periods <input type="text" value="32"/> Semiperiod At '0' [NS] <input type="text" value="46.047"/>																
Port_1	Starts At Logic Level '0' <input type="text" value="0"/>	Number Of Intervals <input type="text" value="5"/>																
<input type="text" value="Generic"/>	Goes From 'X' To '0' After: [NS] <input type="text" value="0"/>	<table style="width: 100%; border: none;"> <tr> <td style="width: 25%;"></td> <td style="width: 25%; text-align: center;">'1' After [NS]</td> <td style="width: 25%; text-align: center;">'1' After [NS]</td> <td style="width: 25%;"></td> </tr> <tr> <td></td> <td style="text-align: center;">'0' After [NS]</td> <td style="text-align: center;">'0' After [NS]</td> <td></td> </tr> <tr> <td></td> <td style="text-align: center;"><input type="text" value="1210.900"/></td> <td style="text-align: center;"><input type="text" value="4601.023"/></td> <td style="text-align: center;"><input type="text" value="4666.324"/></td> </tr> <tr> <td></td> <td style="text-align: center;"><input type="text" value="4681.846"/></td> <td></td> <td></td> </tr> </table>		'1' After [NS]	'1' After [NS]			'0' After [NS]	'0' After [NS]			<input type="text" value="1210.900"/>	<input type="text" value="4601.023"/>	<input type="text" value="4666.324"/>		<input type="text" value="4681.846"/>		
	'1' After [NS]	'1' After [NS]																
	'0' After [NS]	'0' After [NS]																
	<input type="text" value="1210.900"/>	<input type="text" value="4601.023"/>	<input type="text" value="4666.324"/>															
	<input type="text" value="4681.846"/>																	
Port_2	Starts At Logic Level '0' <input type="text" value="0"/>	Number Of Intervals <input type="text" value="1"/>																
<input type="text" value="Generic"/>	Goes From 'X' To '0' After: [NS] <input type="text" value="0"/>	'1' After [NS] <input type="text" value="50.0"/>																

Show Current Stimulus Below

Start Translation

Print The List Of Translated Cells
 Save This Stimulus For Future Uses
 You Can Load An Old Stim To Start From

Total Sim Time [NS] (Time Reference: Start Of Sim)

```

At 0NS: Port_0('0')
At 0NS: Port_1('0')
At 0NS: Port_2('0')
50.0NS After That: Port_2('1')
1160.9NS After That: Port_1('1')
1978.9NS After That: Port_0('1')
45.988NS After That: Port_0('0')
46.047NS After That: Port_0('1')
14 Full Port_0 Periods ('0'->'1') With No Other Events
30.698NS After That: Port_1('0')
15.29NS After That: Port_0('0')
46.047NS After That: Port_0('1')
3.964NS After That: Port_1('1')
15.522NS After That: Port_1('0')
26.502NS After That: Port_0('0')
46.047NS After That: Port_0('1')
45.988NS After That: Port_0('0')
14 Full Port_0 Periods ('1'->'0') With No Other Events
3911NS After That: End of Simulation
                    
```

Proposed methodology (5): Module Generation

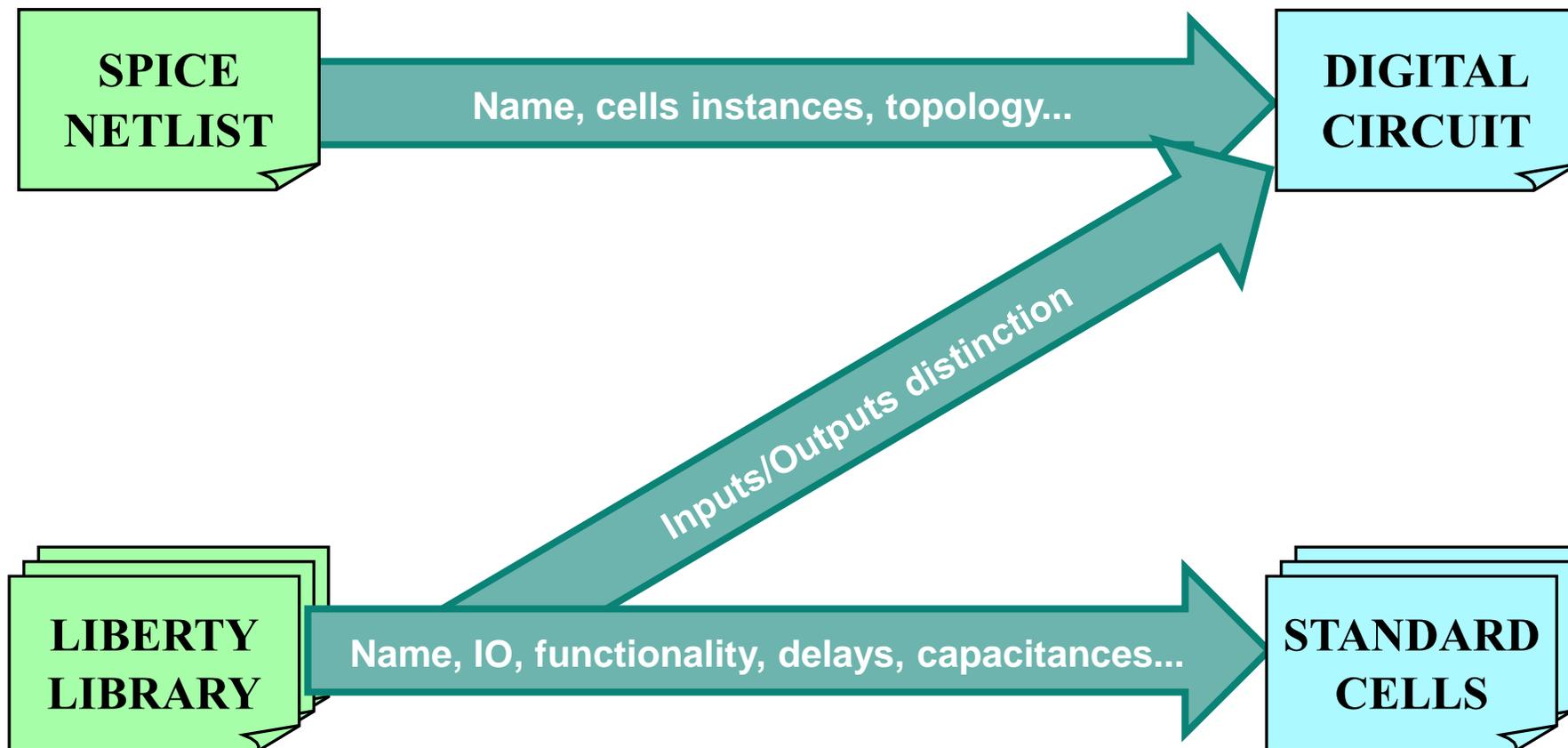
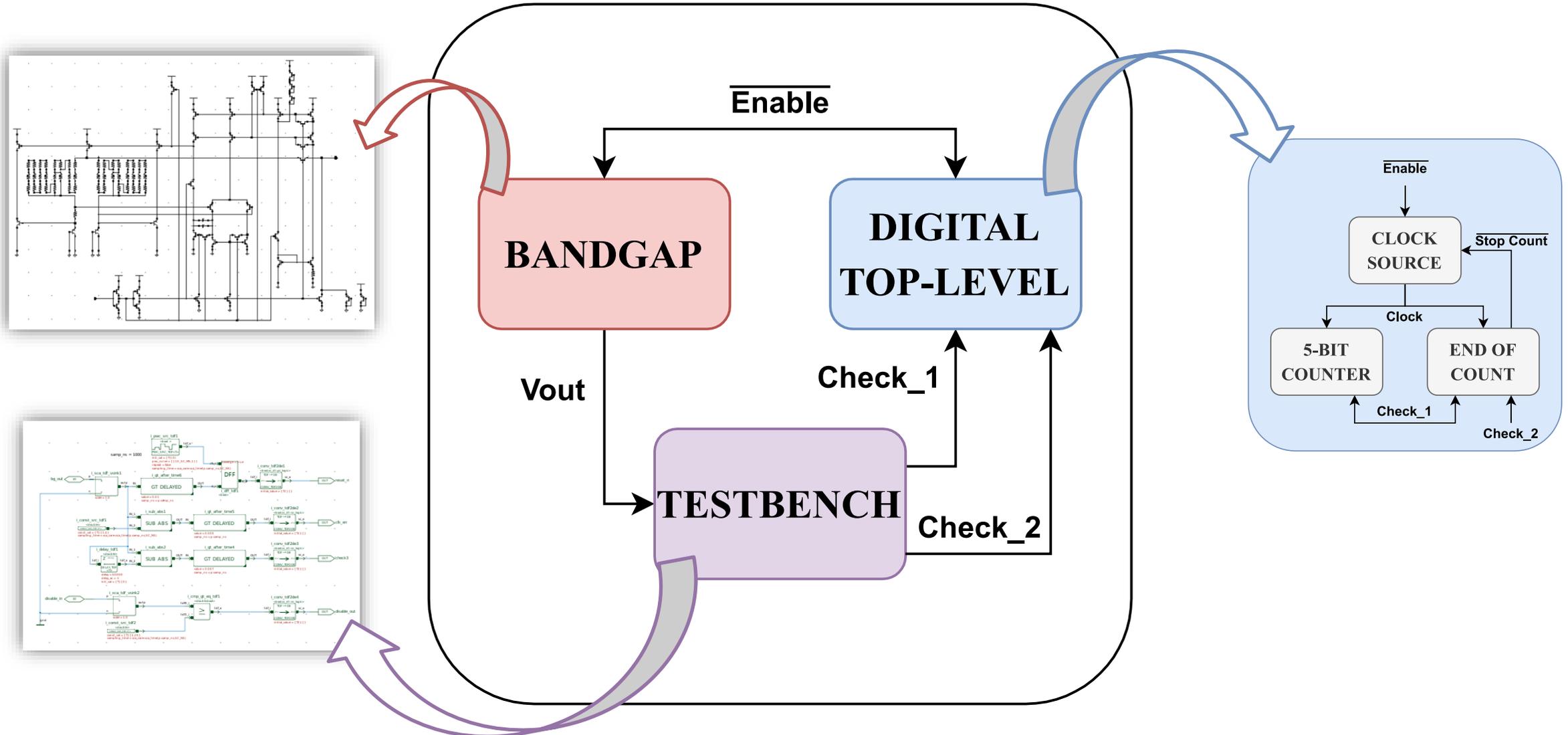


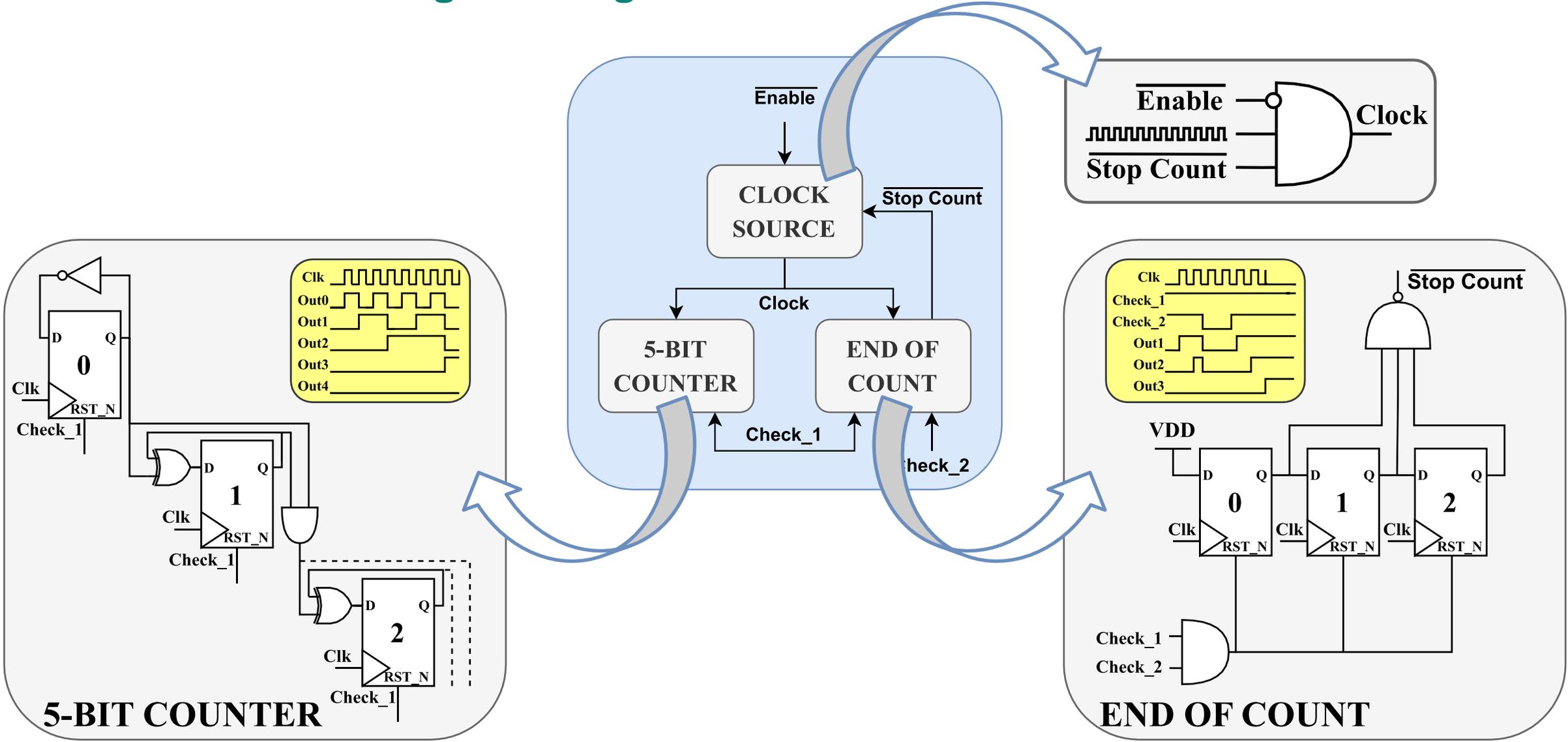
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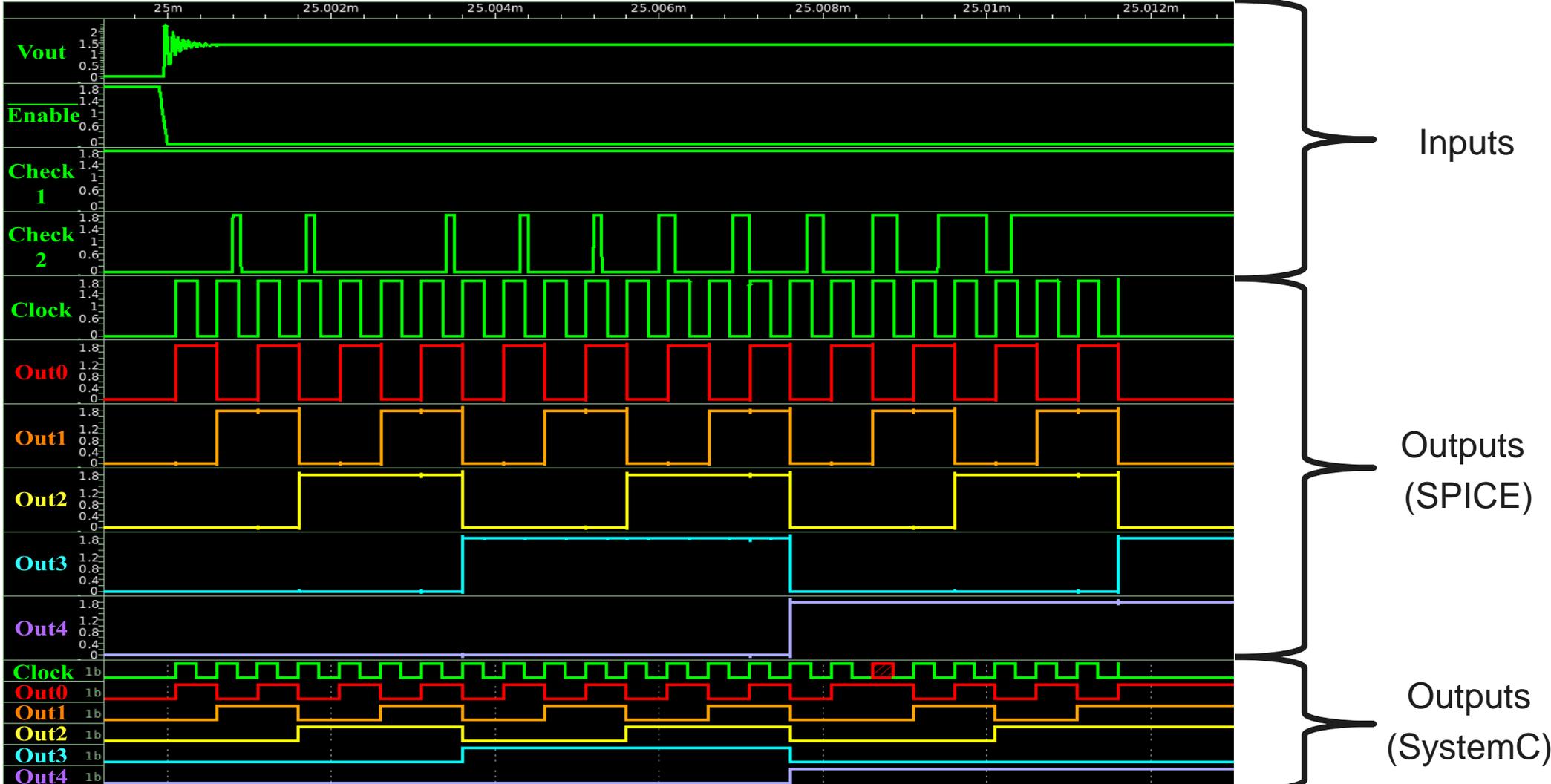
Main Benchmark: Infineon Open-Source Bandgap



Main Benchmark: Integrated Digital Circuit

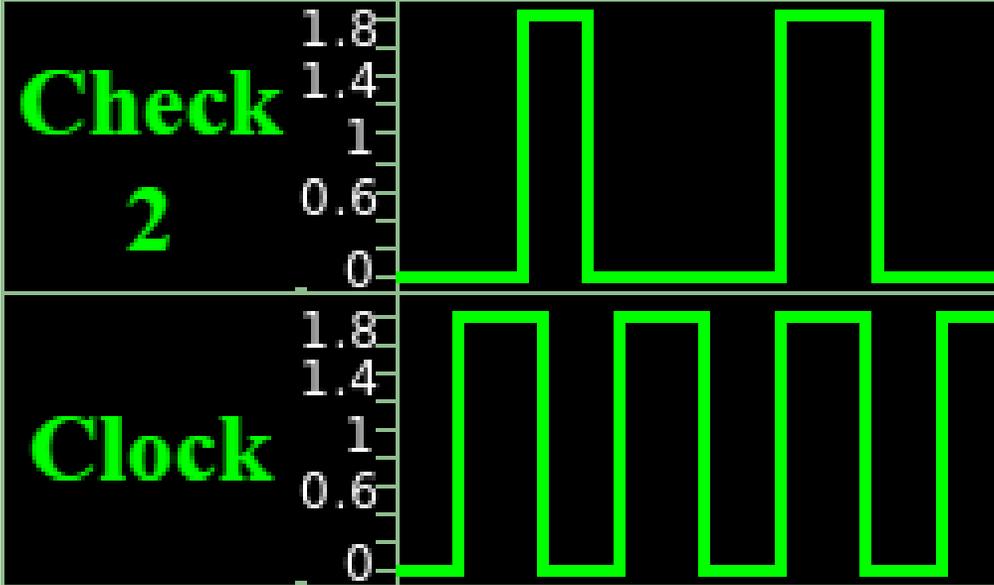


Main Benchmark: Results



Main Benchmark: Results (Zoom)

Cause



Effects

