

SystemVerilog-like Assertions in SystemC

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- Motivation
- Assertions in SystemVerilog
- Challenges
- Assertions in SystemC
- Outlook

Complex Systems

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Verification Environment



- DUV: analog HW, digital HW + control SW
- Directed testing
- Stimuli generation
 - Manual



Not practical!

DUV too complex!!

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Assertion Based Verification Environment

- DUV: analog HW, digital HW + control SW
- Stimuli generation
 - Manual
 - Constrained random
- Monitoring
 - Assertions
 - Coverage



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What are assertions?

Assertions



- Capture the intended behavior of DUV
 - Validate the behavior of a design
- Also referred as properties Executable comments

Is it working correctly?

- Automate validation of the design against the specification.
- Advantages
 - Support better testing and verification
 - Reusable
 - Portability
 - Make debugging easier



Assertions - Example

Required behavior
 If req is high,
 then should be high in next cycle
 AND done is high AND error is low
 one cycle later.







SVA Assertions – Example

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Challenges for Mixed Assertions (1)

How to define time continuous properties?







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How to define frequency response properties?







Challenges for Mixed Assertions (2)

Mixed-signal interface properties E.g., Analog to Digital Converter



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Challenges for Mixed Assertions (3)





All together: mixed assertions



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Mixed ABV

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Requirements

a formal declarative language for expressing properties a mechanism for checking that the DUV

satisfies the properties

What we need

SystemC/AMS assertions language All the building blocks from digital Mixed assertions layer Analog expressions Mixed signal expressions Software expressions





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Mixed Assertions Based Flow - Language



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Application Programming Interface (API)



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Interface/ gateway to a software component Defines how other components or systems can use it Components/systems rely only on the API

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COSIDE Integration



	Search Project SystemC-AMS Tools Run Window License Help	
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	□ Letest_assertions.cpp X	□ □ BE Outline X - Hierarchy □ □ □ ↓ ^a z X X • H · ·
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Assertions	Console X Properties X I Properties	Problems Search & Problems Search is used from the search dialog
output	Warning: trl: Start of sequence in Sequence In file: assertion_test/test_assertions.cpp:102 In process: trl_assertion_tree.trl_process_17 @ 8500 us 9 ms cnt: 19 clk: 1	
	Warning, tr1. Ctart of companyo	

Assertio

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Summary and Outlook



- Assertions lib for SystemC/AMS not available
- Running prototype
- Syntax is work-in-progress
- Closely follow SystemVerilog Assertions
- Analog and mixed-signal interactions



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