From COSIDE® to Cadence®

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Infineon Technologies AG

Agenda

1. History – project background
2. Conversion from Coside to Cadence – WHY?
3. Problems and Shortcomings
4. The brighter future

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History – project background (1/2)

› Infineon's Radar Success Story

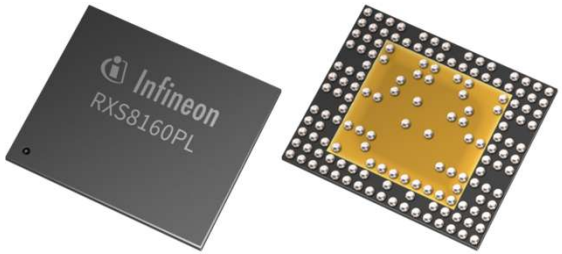
2003 - 2006:
- 77GHz 2RX 2TRX + VCO Prototype

2009:
- series Product (Porsche Panamera)

2012:
- SiGe:C & CMOS Companion

2014:
- BiCMOS Integration

2016:
- Full Integration of RF-IF-ADC-Digital Interface



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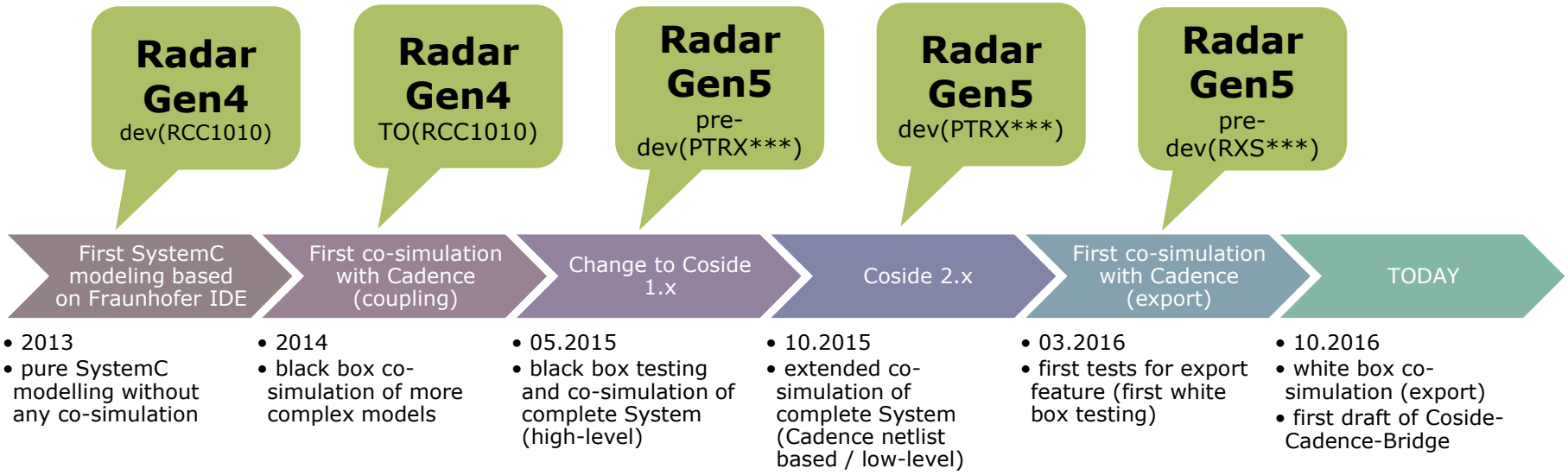
History – project background (2/2)



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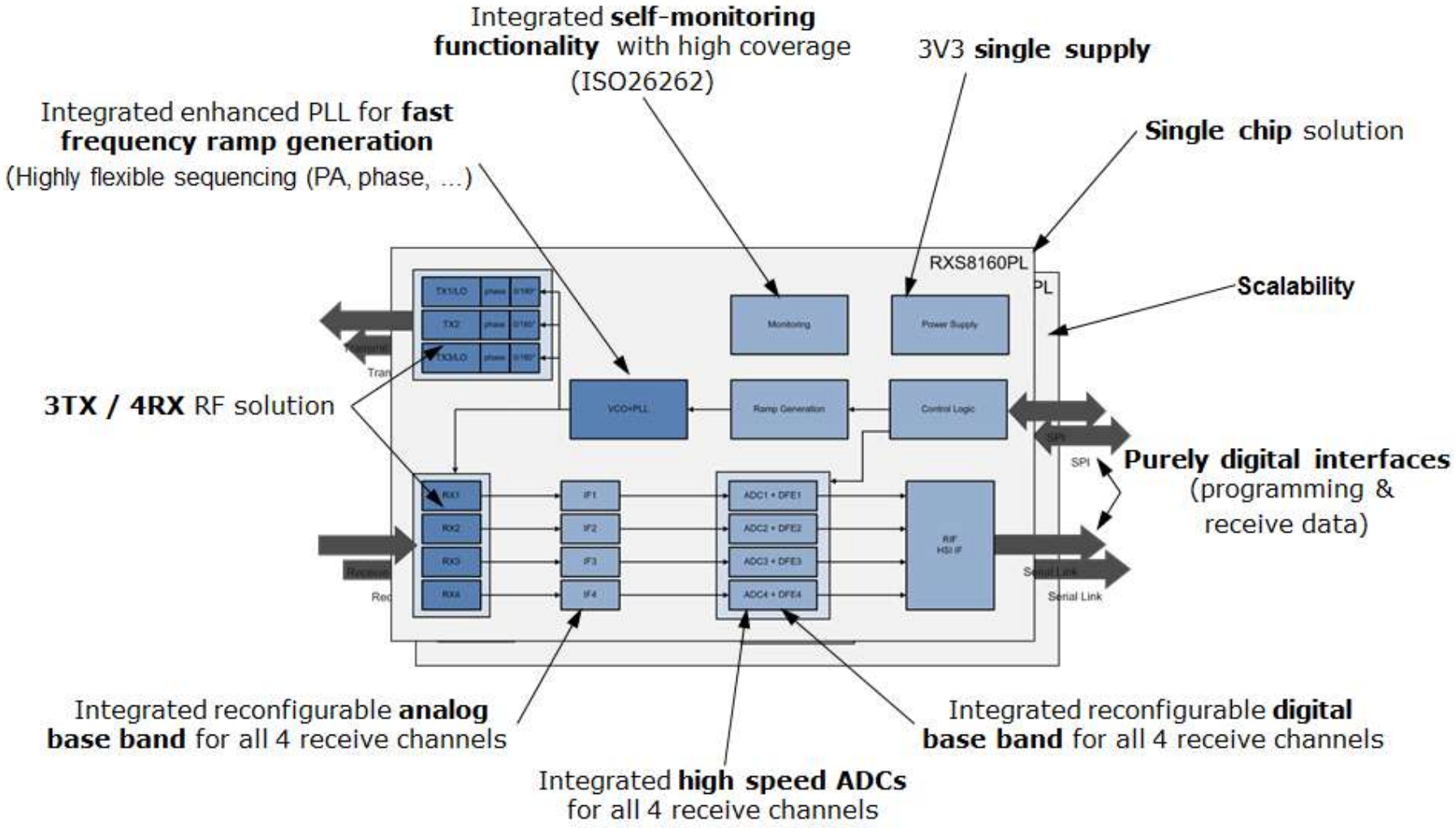
From Coside to Cadence – WHY? (1/4)



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From Coside to Cadence – WHY? (2/4)

› Increased complexity

› Demanding customers

› Faster time to market

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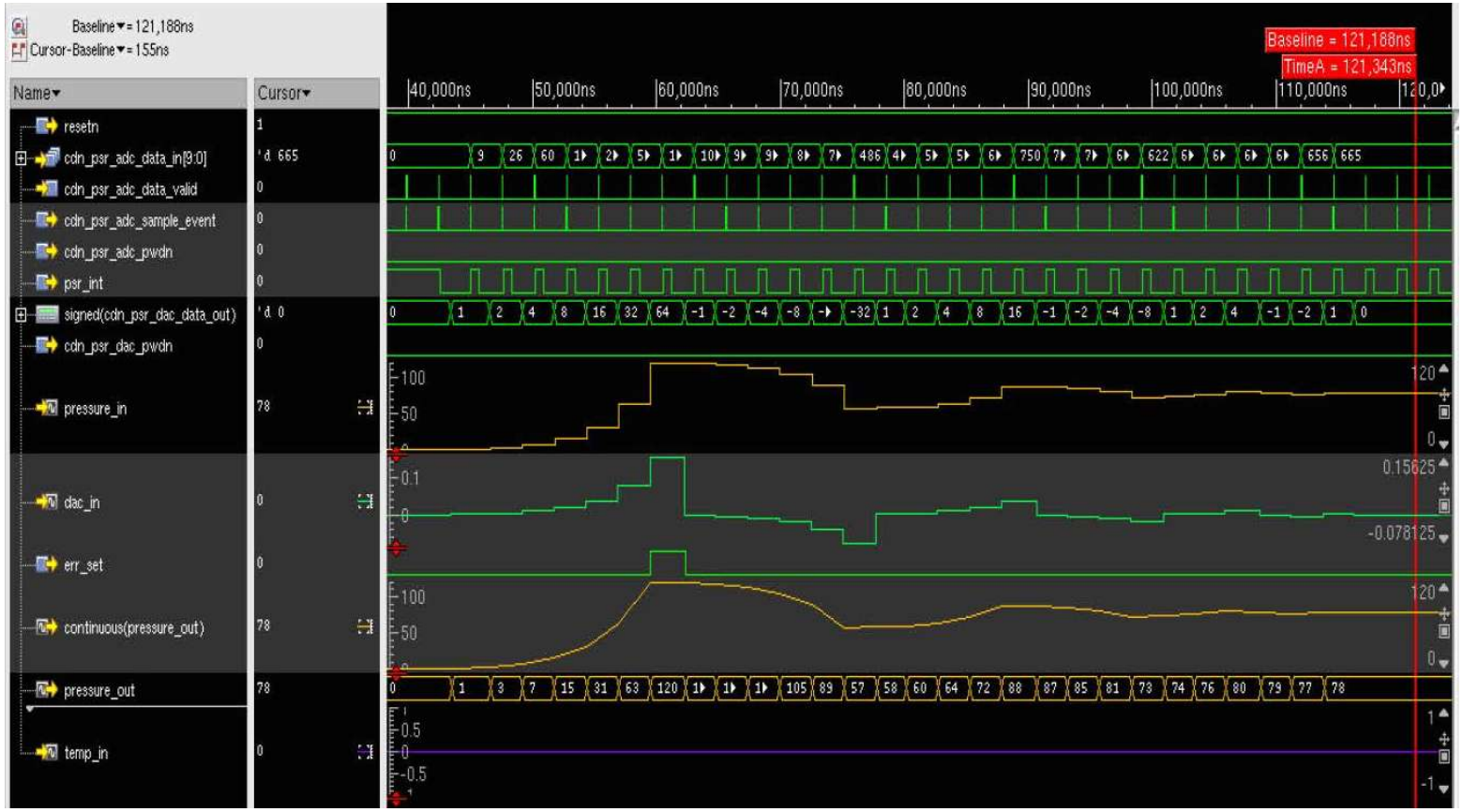
From Coside to Cadence – WHY? (3/4)

› Enabling transient co-simulations on system level



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From Coside to Cadence – WHY? (4/4)

- Reduction of simulation time
  - Simulation of PLL

SystemC	Cadence Spectre	Matlab
VCO = 2.6GHz; resolution 83ps; 700us sim time		

- Higher quality of design
  - Use SystemVerilog UVM methodology on System-Level with SystemC models for analog and “real” RTL for digital

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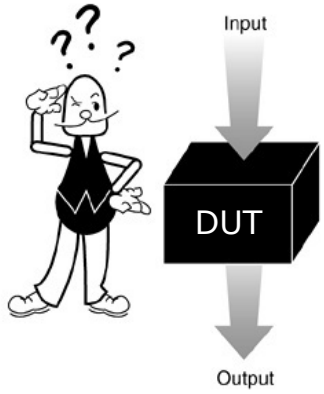
Debugging of SystemC Models in Cadence

- Using the coupling method to export SystemC models from Coside leads to a “BLACK-BOX”



Black-Box Testing

  - No internals of model visible in Cadence
  - Multiple instances not easily possible with shared-objects
  - Bug fixing needs many iterations
  - Conversion issues within connect modules (CMs) are hard to find

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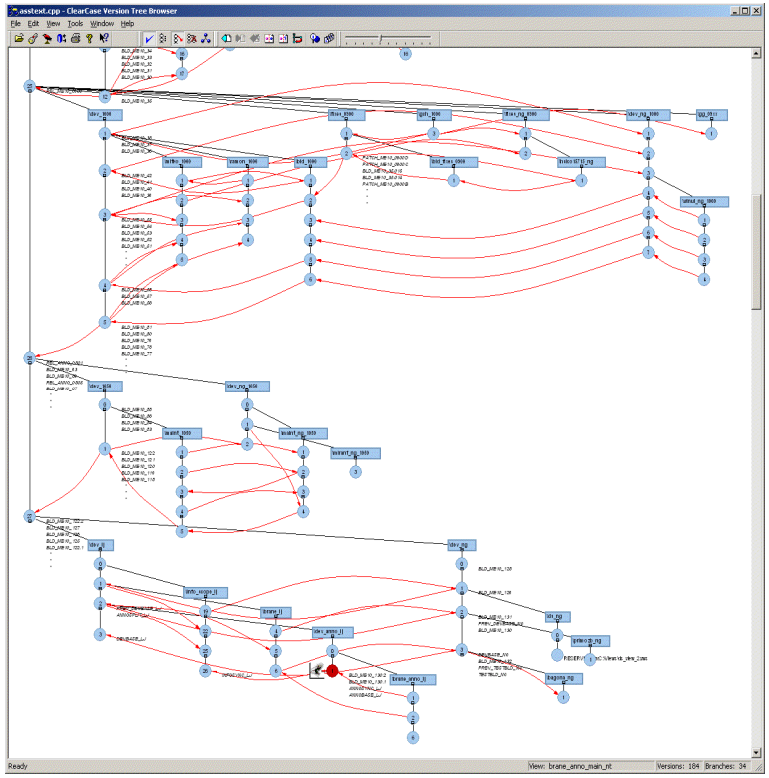
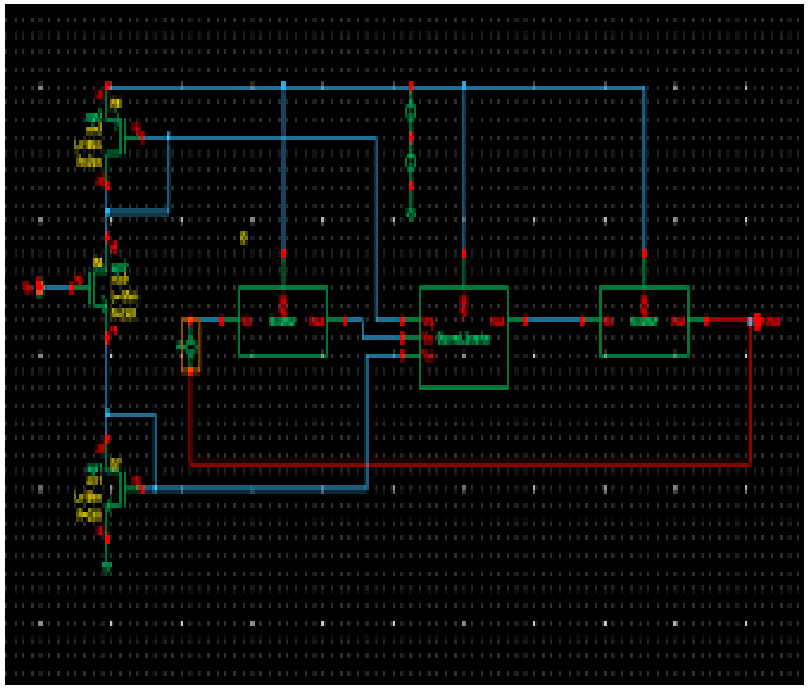
“Problems” with Cadence and SystemC / Coside

- Keep the design data between Cadence and Coside consistent
  - Cadence uses OA database
  - ClearCase is also not helpful
  - Analog design data is schematic based
  - Changes hard to find





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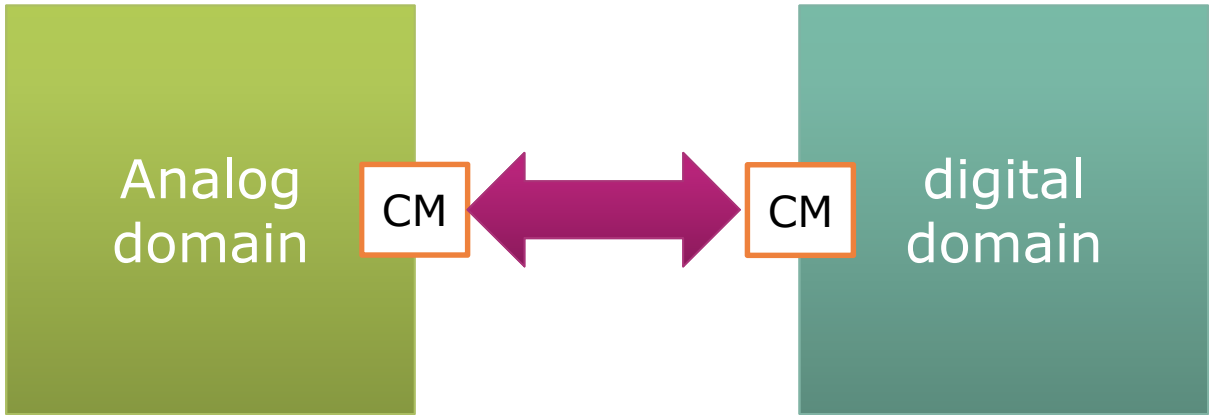
Interaction between different domains (1/2)

- Data exchange between analog and digital is only possible with "special" conversion cells – connect modules (CM)
  - Insertion shall be / is done automatically
  - no schematic changes / manual insertion allowed



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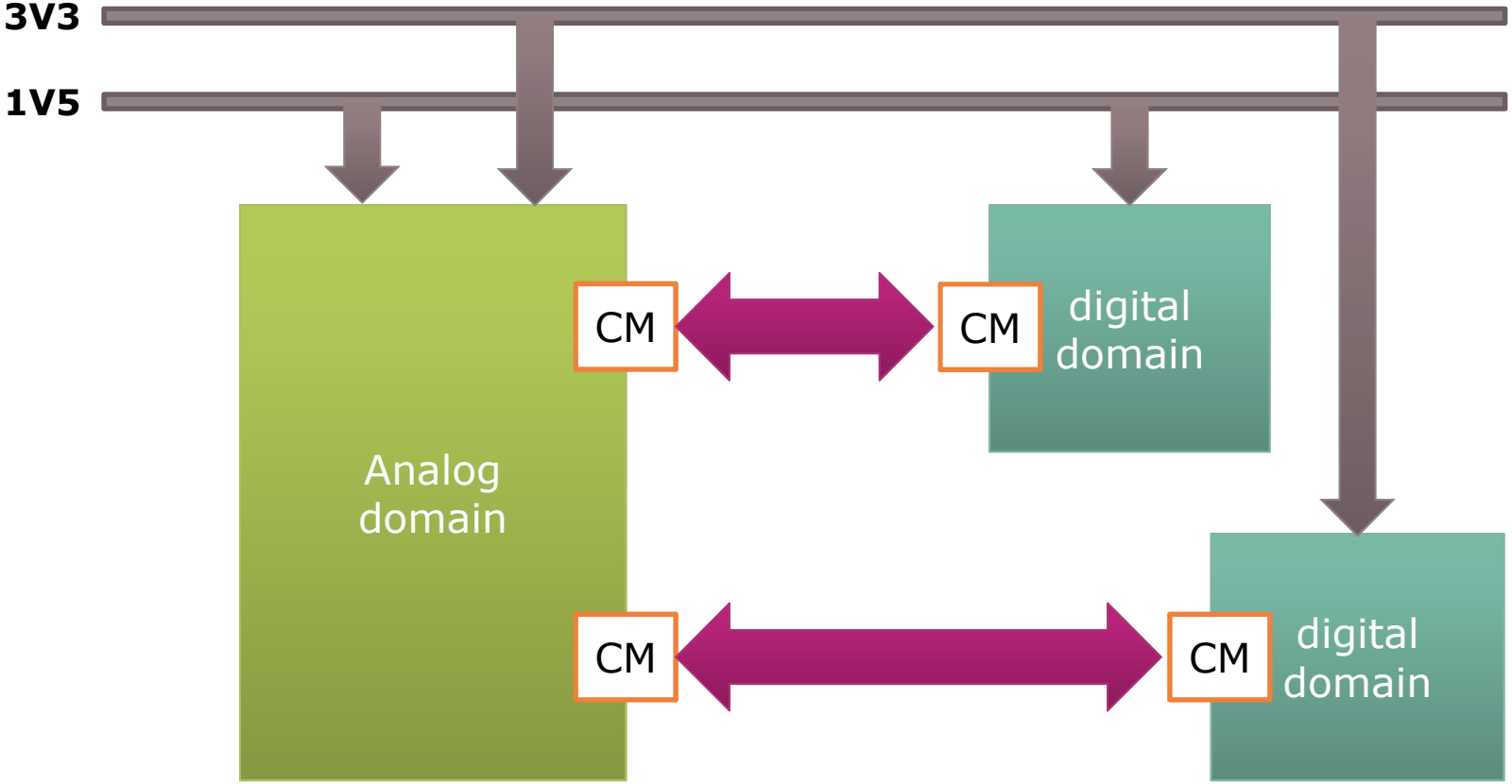
Interaction between different domains (2/2)

- More problems with multi-voltage designs
  - How to define voltages for CMs?
  - Handwritten VAMS wrapper necessary (supply aware)



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“Problems” with complex designs

- Interaction between different languages
  - **Digital**: Verilog / VHDL
  - **Analog Models**: SystemC / C++ / Verilog-A / Verilog-AMS
  - **Top-Level TB**: SystemVerilog / Specman
  - **Analog**: spice

- Interaction between different simulators
  - **Digital**: INCISIVE / NC-SIM
  - **Analog**: Spectre / Ultrasim / P-Spice
  - **SystemC Kernel**: C++

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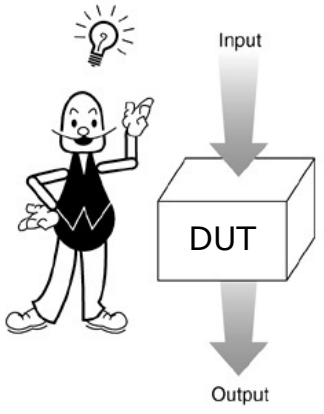
White-Box integration in Cadence

- Use Cadence gcc + kernel to integrate SystemC models in the AMS co-simulation
  - Coside offers a “make” based solution to generate a white-box module for Cadence

make
- Compiles modules using Cadence
- Generates a irun-scripts & resource files

irun
- Compiles a module to .pak & .so
- Additional .res file can be used in AMS-Simuation

ncsim
- Loads .res file to identify available modules
- Simulates SysC modules a white-box instances



White-Box Testing

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From hand-made to generated (1/3)

- Supply aware VAMS wrapper must be generated based on available design information

- **Needed Information:**
  - Block / module supplies
  - Related supplies for ports
  - Custom defines for AMS-Simulator

- **Solution from Coseda:**
  - Add all necessary information as port / schematic VAMS-attributes
  - Attributes are inherited through hierarchies

- **Drawback:** Data insertion in Coside might become a little tricky for bigger designs. Is there a better way? → YES

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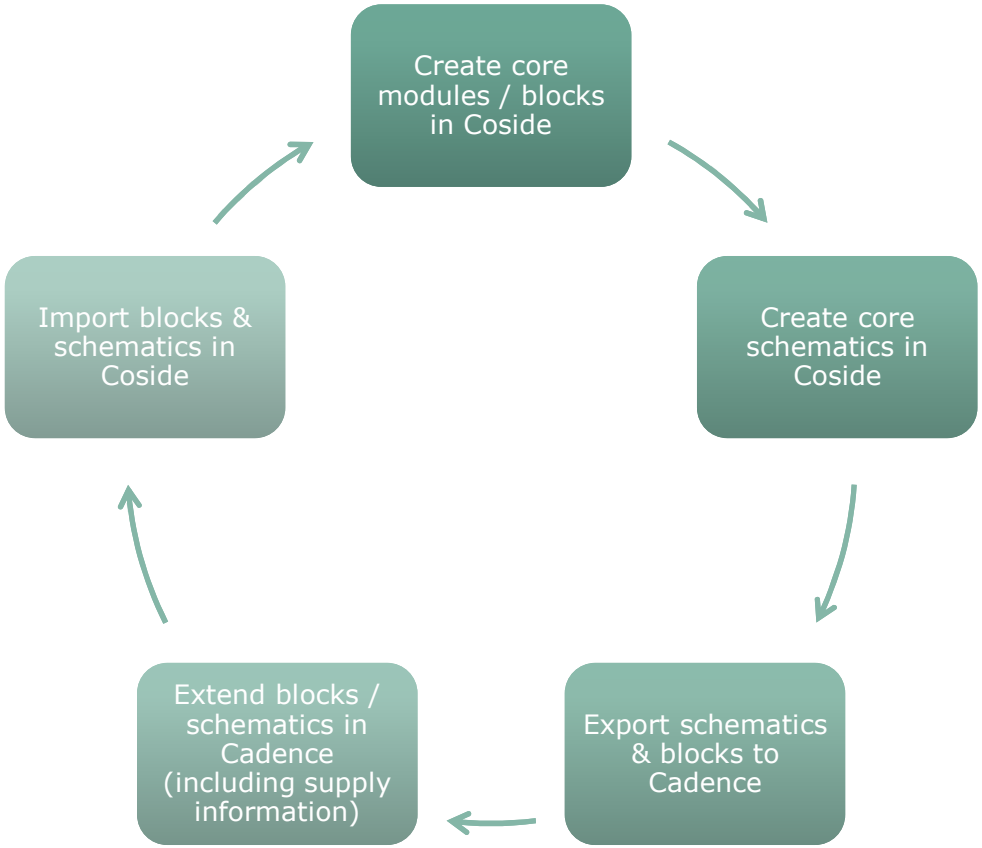
From hand-made to generated (2/3)

- The better way to insert power supply information
  - Use the export / inport feature from Coside to exchange data and attributes between Coside and Cadence (Coside-Cadence-Bridge)



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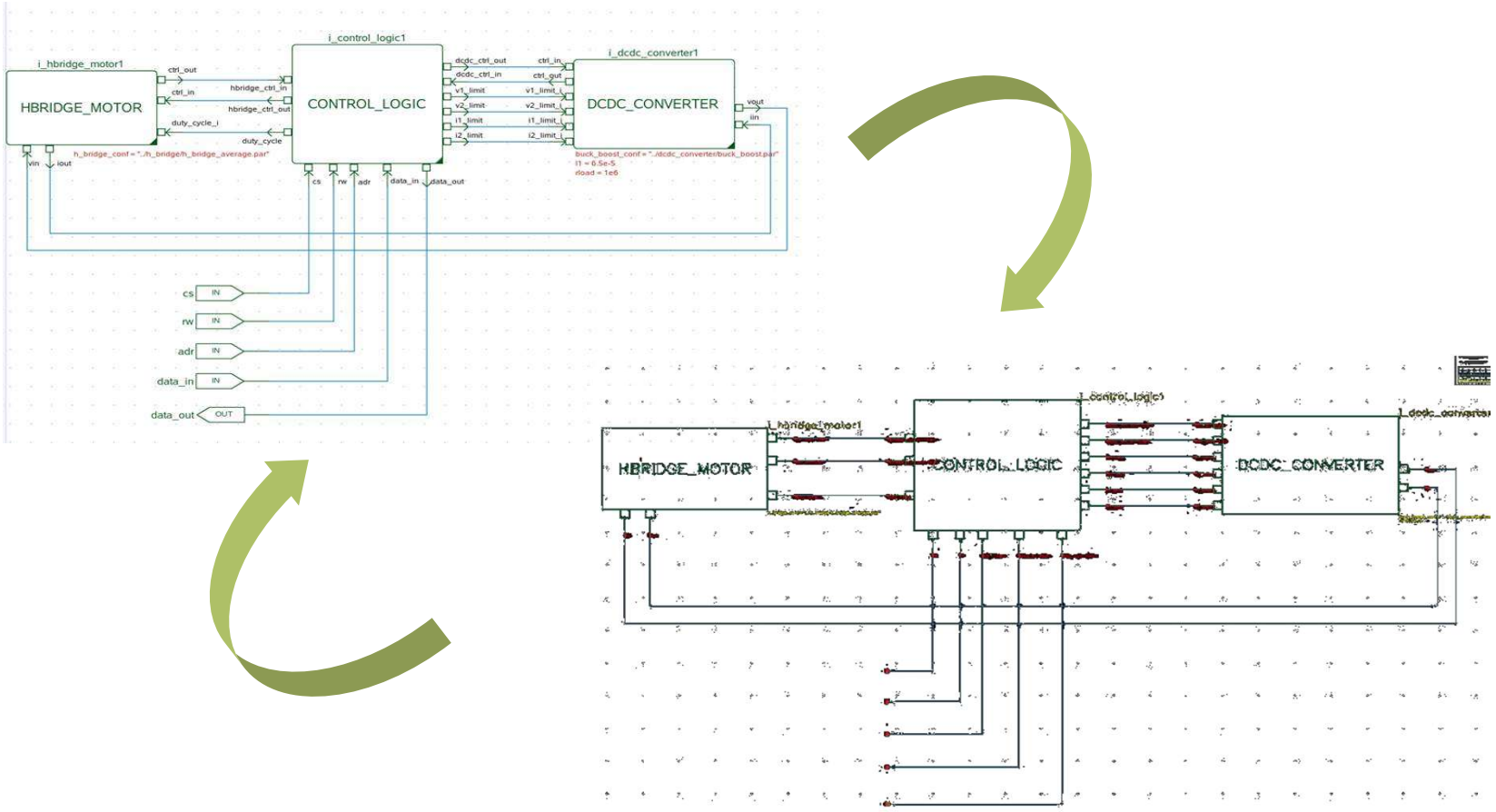
From hand-made to generated (3/3)

› Schematic & block conversion from / to Coside / Cadence to keep data in sync



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Q&A

› Questions?

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Conclusion

- Coside / SystemC helps us during the development of bigger designs to achieve
  - Better quality of the system
  - Faster development cycle

- There is still room for improvement

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