ANALOG IP – WITH INTELLIGENT IP FROM SYSTEM TO SILICON

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Analog IP – with Intelligent IP from system to silicon

- What is Intelligent IP (on silicon level)?
- Intelligent IP bottom-up: from silicon to system level
- Intelligent IP top-down: from system level to silicon
Our VISION
Intelligent A/MS IP (IIP)

Offering innovative A/MS IP which are

- **flexible** as software, processors, memory compilers or soft IP
- **configurable** by a wide range of different parameters
- generated in a few seconds to minutes
- **verified on different technologies** in a strictly standardized way
Intelligent IP
A novel approach for analog and mixed-signal IP

Easy-to-use through...
- Intuitive graphical interface
- Seamless design tool integration

Full design data ...
- Automatically generated
- Can be altered “as usual” (non-proprietary)

Flexible through...
- Technology-generic IIP description
- Automated configuration

+ testbenches, simulation states
+ integration model
+ system behavioral model

XFAB 180nm
AMS 180nm
GF 40nm
GF 28nm
ST 28FDSOI
GF 22FDX
Intelligent IP
Productive application examples & benefits

- Initial IIP development in 4 weeks (2x speed up)
- Layout generation: ~10 min (>1000x speed up)
- Regeneration (e.g. for 10 bit resolution): ~3 min
- Design trade-offs by back bias control
- Silicon available

80MSps 12-bit DAC in STM 28nm FDSOI

- IIP reuse for tech node shrinking (4x speed up)
- Layout generation: ~5 min (>1000x speed up)
- Regeneration for new target: ~5 min
- Design trade-offs by body bias control
- Silicon available in Q3/2017

500MSps 10-bit DAC in GF 22FDX
Intelligent IP

Use case Configurability for new product requirements

Configuration of ADC resolution & Pipeline arrangement

- 12-bit
- 10-bit
- 8-bit

Configuration of Sampling rate & Power budget

- 100 MSp
- 40 MSp
- 4 MSp

Ready for multiple technology requirements

- 22nm FDSOI, 28nm FDSOI, 28nm, 40nm, 180nm, … for different fabs

System-level configurability in addition to expert mode input parameters
Intelligent IP supports electrical requirement flexibility on different levels:

**Primitive level**
Design parameter, primitive change, ...

**Functional level**
Bandwidth, gain, ...

**System level**
INL, ENOB, resolution...
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Intelligent IP
bottom-up: from silicon to system

- System design
- Implementation

Intelligent IPs
(executable, configurable, transistor-level verified)
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Intelligent IP

top-down: from system to silicon (1)
Intelligent IP
top-down: from system to silicon (2)

System design

System C library:
(configurable)

Re-generation & verification

IIP

ADC 1
spec 1
spec 2
spec 3

ADC 2
spec 1
spec 2
spec 3

ADC 3
spec 1
spec 2
spec 3

Sub block 1
Sub block 2
Sub block 3

Design Space

ADC 1
spec 1
spec 2
spec 3

ADC 2
spec 1
spec 2
spec 3

ADC 3
spec 1
spec 2
spec 3

1 2 3
Intelligent IP
top-down: from system to silicon (3)

- System design
  - System C library: (configurable)
  - ADC 1, ADC 2, ADC 3
- Implementation
  - IIP
    - ADC 1
      - spec 1
      - spec 2
      - spec 3
    - ADC 2
      - spec 1
      - spec 2
      - spec 3
  - New IP design
  - Sub block 1
  - Sub block 2
  - Sub block 3
- Design Space
  - Spec 1
  - Spec 2
  - ReUse of IIPs
    - ADC 1
    - ADC 2
    - ADC 3

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Conclusion

- Intelligent IP provides automated design of analog IPs & is in productive use

- Generation of system models in development

- Goal: provide configurable SystemC model library in Coside for
  - exiting verified A/MS-IPs
  - A/MS-IPs, which can be re-generated and verified quickly
  - A/MS-IPs, which can be quickly designed using Intelligent IP technology

- Request: discussion on customer problems and expectations
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